3. Assembling technologies - classical and based on RoHS&WEEE European Directives

3.1 Chip packaging technologies

As the electronics industry has become more consumer-product-oriented, cost has become more important even for high-performance products. The required portability of consumer products has also increased the importance of size, driving reduced pitch for interconnections. From mobile telecommunications and satellite broadcasting to aerospace and automotive applications, each imposes its own individual demands on the electronic package.

The development of the IC/microsystem package is a dynamic technology. Applications that were unattainable only a few years ago are today common place thanks in part to advances in package design. Advancements in materials technology allow semiconductor manufacturers to improve the functionality and reliability of electronic systems and gadgets. The importance of materials technology is especially apparent in the packaging segment of the semiconductor industry, where the packaging materials market is estimated to be 5-6 times larger in revenues than the size of the assembly and packaging equipment market. The innovation that is required of semiconductor makers and packaging subcontractors is exciting when one examines all the new package form factors and new materials that are now available or being developed. Advancements, such as system-in-a-package (SiP), package-on-package (PoP), wafer-level packaging (WLP) and through-silicon vias (TSV), are changing how devices are thinned, die attached, wire bonded (or interconnected) and encapsulated. These packaging technologies are material and process driven and, as such, there have been a number of new materials developments, from new substrate resins to smaller diameter wires, to address various challenges. Chip-scale packaging (CSP), flip-chip packaging (FCP) and various SiP technologies require organic substrates, new mold compound formulations, smaller diameter wire and, for some packages, customized underfill materials. Packaging technology delivers solutions for integrating multiple devices and increasing the functionality of electronic devices. The semiconductor industry is in the era of 28nm process, and it is expected that it will meet 16/14nm around 2020 and 10/7nm in 2025 (figure 3.1.1). New materials technology will be critical in further enabling innovation in a cost-driven marketplace. An overview of the chip packaging is presented below (figure 3.1.2).

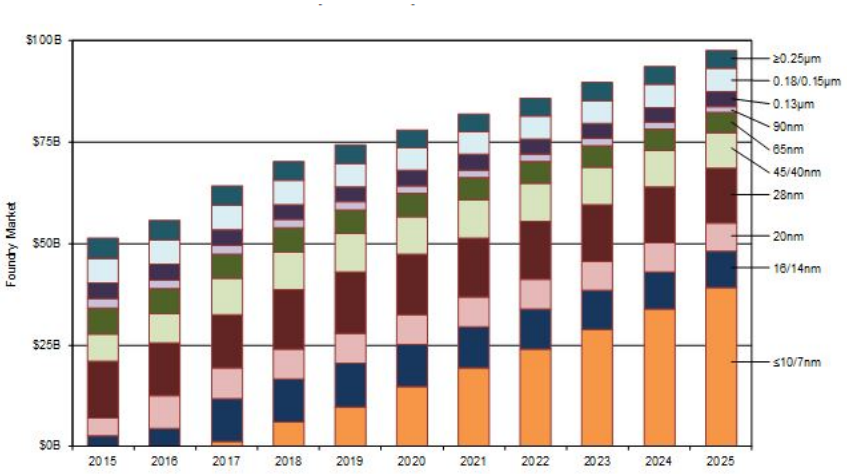


Fig. 3.1.1 The foundry market by feature dimension (Dr. Handel Jones, "Semiconductor Industry from 2015 to 2025", International Business Strategies (IBS))

MicroElectroMechanical System (MEMS) is a relatively new field which is tied so closely with silicon processing that most of the early packaging technologies will most likely use existing packaging from the semiconductor microelectronics field. The package provides the interface between the components and the overall system and serves to integrate all of the components required for a system application in a manner that minimizes size, cost, mass and complexity.

As an application of MEMS see the animation from below presenting the virtual MEMS button and its assembling starting from:

- micro-batteries;
- sensor modules;
- solar cells;
- plastic, transparent, cover.

Virtual MEMS button (http://www.youtube.com/watch?v=PtYQeRjTEuU)

There are three main functions of the MEMS package:

♦ mechanical support: protection from thermal and mechanical shock, vibration, high acceleration, particles and other physical damage during storage and operation according to the mission or application; the coefficient of thermal expansion (CTE) of the package should be equal to or slightly greater than the CTE of silicon in order to avoid die cracking and delamination;

♦ electrical connection to other system components: transfer of DC power, RF signals (in some designs); the final connection between the MEMS and the DC and RF lines is usually made with wire bonds, although flip-chip die attachment and multilayer interconnects using thin dielectric may also be possible;

♦ protection from the environment: moisture, corrosion can damage MEMS devices. Protection has to take into account the functionality of the MEMS device (e.g. some devices have to measure concentrations of certain types of liquids) in order to opt for a simple (mechanical) protection or a traditional (hermetic or non-hermetic) protection. MEMS packages for high reliability applications may need to be hermetic with the base, sidewalls, and lid constructed from materials that are good barriers to liquids and gases and do not trap gasses that are later released.

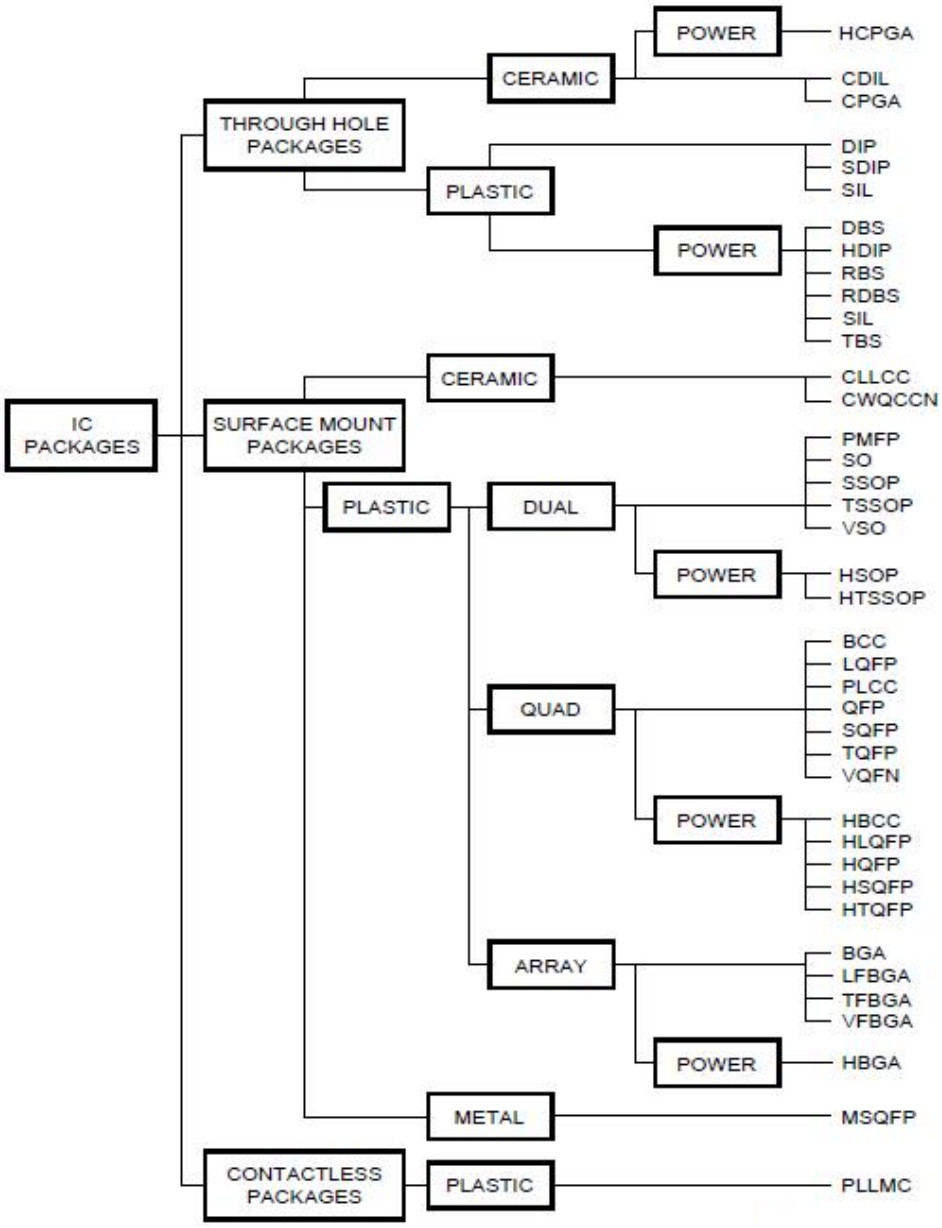


Fig. 3.1.2 An overview of the chip packaging

The packaging industry has become increasingly important since 2000, and the debut of BGA, FC and CSP has sped up the progression of semiconductor industry. However, the front-end of semiconductor manufacturing has been in stagnancy, still in the era of 12-inch wafer, and it is likely that 18-inch wafer era will come shortly. The largest wafers made have a diameter of 450mm (18 inch) but are not yet in general use.

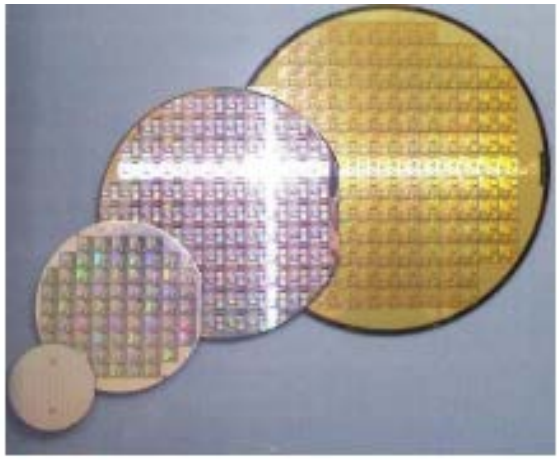


Fig. 3.1.3 2-inch, 4-inch, 6-inch and 8-inch silicon wafers used in semiconductor manufacturing processes (source: The Move to the next Silicon Wafer Size: A White Paper from the European Equipment and Materials 450mm Initiative (EEMI450))

Currently, a revolutionary packaging, TSV packaging, presents itself as the so called 3D IC. The technology will dramatically improve chip transistor density, cubic density rather than plane density, and make semiconductor industry surpass the development pace of Moore's Law ("the number of transistors that can be placed inexpensively on an integrated circuit doubles approximately every two years"). Not only packaging companies and wafer OEMs, but also nearly all global prominent semiconductor companies such as IBM, Samsung, Intel and Qualcomm are all actively developing TSV technology. TSV has been in large shipment in image sensor and MEMS field, and it has rapidly expanded to memory field, and to DSP, RF IC, cell phone baseband, processor, CPU and GPU. Commercial applications continue to emerge for sensors, memory, and FPGAs.

Japan and Taiwan have almost dominated IC packaging industry. Among the global top 12 companies, seven are from Taiwan, two from Japan, two from the United States, and one from South Korea.

The semiconductor industry is a cornerstone of today's high-tech economy, supporting over 100,000 direct and even more indirect jobs in Europe. This position has been achieved through continued miniaturization in complementary metal-oxide-semiconductor (CMOS) technology, which will only last for a maximum 10-15 more years. In line with its Lisbon Strategy, the European Commission (EC) has identified an urgent need to assess possible technology solutions for the "Beyond CMOS" era to meet the challenges of global competition. The major ICT Information and Communications Technology) challenge is to find alternatives for information processing and storage beyond the limits of existing CMOS. Graphene, ultra-thin layers of carbon, is particularly promising due to its novel electronic properties. Initial data indicates that graphene is a prime candidate for "Beyond CMOS" switches and interconnects, and is, despite its revolutionary nature, complementary to conventional CMOS.

Currently, in spite of such many types of packages, there are available only four ways for interconnection of the chip to the rest of the world: wire bonding, tape automated bonding, flip chip and laser.

3.1.1 Wire Bonding (WB)

Basics

Wire-bonding is an electrical interconnection technique using thin metallic wire and a combination of heat, pressure and/or ultrasonic energy (figure 3.1.4). This technology originated with AT&T's beam lead bonding in 1950s. It is generally considered the most cost-effective and flexible interconnect technology and is used to assemble the vast majority of semiconductor packages (wire-bonding accounted for well over 90% of all the chip-to-package interconnections formed in 1999).

A brief history of wire-bonding is presented below:

1957 - Bell Labs was the first to publish information regarding wire-bonding;

1959 - J.W. Beams reported his characterization of metallic thin film strength;

1971 - Nowaskowski & Villela found three variations of power cycling tests;

1972 - Horsting publishes "Purple Plague and Gold Purity", describing contamination based void formation in inter-metallic layers;

1972 - Ravi & Philofsky: Machine for accelerated tests of various wires;

1973 - Ravi & Philofsky published a failure prediction model of thin films;

1973 - C.N. Adams developed a model for wire failure near ball bond;

1974 - G. Harman sited cause as manufacturing defects or environmental stresses;

1989 ~1991 - M. Pecht & A. Dasgupta models for wire flexture, pad & wire & substrate shear, and axial tension;

2000 – Ramminger's work on under-wedge cracking.

The cost analysis reveals that the main cost of wire-bonding method includes:

- Wire-bonder;
- Die attach equipment;
- Support equipment, such as wire pull and shear stations, plasma etchers, as well as storage facilities;
- Materials including tool, wire, die attach materials;
- Engineering.

Wire-bonding is a solid phase welding process, where the two metallic materials (wire and pad surface) are brought into intimate contact. Once the surfaces are in intimate contact, electron sharing or interdiffusion of atoms takes place. Heat can accelerate interatomic diffusion, thus the bond formation. In wire-bonding process, bonding force can lead to material deformation, breaking up contamination layer and smoothing out surface asperity, which can be enhanced by the application of ultrasonic energy.

Fig. 3.1.4 Wire-bonding of IC to ceramic package

The advantages of wire-bonding are:

- Highly flexible chip-to-package interconnection process;
- Low defect rates or high yield interconnection processing (40-1000ppm);
- Easily programmed or taught bonding cycles;
- High reliability interconnection structure;
- Very large industry infrastructure supporting the technology;
- Rapid advances in equipment, tools, and materials technology.

As disadvantage, it should be noted that there is a limitation for the application of wire-bonding method due to the fact that terminals of chips have to be arranged at the periphery of the chips, otherwise short circuits are easily caused. Therefore, wire-bonding technique is difficult for high I/O (>500) interconnections.

Wire-bonding is a low cost process since no chip modification is needed, the equipment has an established base of competitive development and substantial non-recurring engineering charge and tooling charge are minimized.

Materials

Referring to materials for wire-bonding, there should be taken into consideration two elements: bond-wire and pad finish.

Bond-wire. In order to obtain a proper wire-bonding, it must be taken into account the electrical and mechanical characteristics of the bonded materials, such as wire material, wire diameter, electrical conductivity, shear strength, elastic modulus, Poisson's ratio, coefficient of thermal expansion. Bond-wires usually consist of one of the following materials - aluminium, copper or gold. Wire diameters start at 15µm and can be up to several hundred micrometres for high-powered applications.

Gold wire is used extensively for thermo-compression bonding and thermosonic bonding. Pure gold can usually be drawn to produce an adequate breaking strength (ultimate tensile strength of the wire) and proper elongation (ratio of the increase in wire length at rupture to the initial wire length given as a percentage) for use as bond wire. Ultrapure gold is very soft, therefore small amounts of impurities such as 5-10ppm by weight of Be or 30-100ppm by weight of Cu are added to make the gold wire workable. Be-doped wire is stronger than Cu-doped wire

by about 10-20% under most conditions, thus advantageous for automated thermosonic bonding where high-speed capillary movements generate higher stresses than in slow or manual bonders.

Pure aluminium is typically too soft to be drawn into a fine wire. Therefore, aluminium is often alloyed with 1% Si or 1% Mg to provide a strengthening mechanism. At room temperature, 1% silicon exceeds the solubility of silicon in aluminium by a factor of 50, which leads to silicon precipitation. The number and the size of the silicon precipitates are dependent on the cooling rate from higher temperatures. Slower cooling rates result in more precipitation and large non-uniform silicon nodules, while faster cooling rates do not allow sufficient time for silicon precipitation resulting in uniformly dispersed nodules. Silicon grain size can affect wire ductility, the second phase can become a potential nucleation site for fatigue cracks.

When alloyed with 1% Mg, aluminium can be drawn into a fine wire that exhibits a breaking strength similar to that of Al-1% Si. The Al-1% Mg alloy wire bonds satisfactorily and is superior to Al-1% Si in resistance to fatigue failure and to degradation of ultimate strength after exposure to elevated temperatures. These advantages of Al-1% Mg wire occur because the equilibrium solid solubility of Mg in Al is about 2% by weight, and thus at 0.5-1% Mg concentration there is no tendency towards second-phase segregation as is the case with Al-1% Si.

Copper-ball bonding to IC metallization has the advantage of economy and resistance to sweep (tendency of the wire to move in the plane perpendicular to its length) during plastic encapsulation. However, a major problem for this system is the bondability. Copper is harder than gold and aluminium, which can lead to cratering or pushing the metallization aside. Therefore a harder metallization is required. In addition, the ball bonding must be performed in an inert atmosphere as copper oxidizes readily.

Pad finish. The pad material properties include conductivity, bondability, activity to form intermetallic phases and Kirkendall voids, hardness, corrosion resistance, coefficient of thermal expansion. In wire-bonding process, different pad metallizations are used (bare Cu, Ag, Ni, Au, Al), depending on the production requirements. Therefore, different metallurgical systems can be formed with different reliability behaviours. The typical metallurgical systems are (wire - pad): Au – Au, Au – Al, Au – Cu, Au – Ag, Al – Al, Al – Ag, Al – Ni, Cu – Al.

Gold wire bonded to a gold bond pad, as well as aluminium-aluminium wire bond system are extremely reliable because the bond is not subject to interface corrosion and intermetallic formation. Even a poorly welded gold-gold bond will increase in strength with time and temperature. Gold wire welds best with heat although cold ultrasonic Au-Au wire bonds can be made (either thermo-compression or thermosonic bonds are easily and reliably made). Aluminium wire on aluminium metallization welds best ultrasonically, although a thermo-compression bond can be produced by high deformation. Thermo-compression bondability, however, is strongly affected by surface contamination.

A very reliable bonding too (for a very long time at high temperatures) is the Au-Ag wire bond-system because it does not form intermetallic compounds and does not exhibit interface corrosion. Gold-wire bonds to silver-plated lead frames have been successfully used in high

production for many years. Bondability problems can be caused by contaminants like sulphur. Thermosonic Au-Ag bonding is usually performed at high temperatures (approximately 250°C) which dissociates thin silver-sulphide films thus increases bondability of silver.

The most commonly used in wire-bonding process is Au-Al welding system. However, this bonding system can easily lead to formation of Au-Al intermetallic compounds and associated Kirkendall voids (voids formed at the boundary interface of an alloy to metal bonding). The formation can be accelerated with the temperature and time of the operational life. There are five intermetallic compounds: Au_5Al_2, Au_4Al, Au_2Al, AuAl, and $AuAl_2$. Therefore, this system often presents a problem in reliability of the bonds.

Intermetallic phases and Kirkendall voids are common for other two systems: Au–Cu and Al-Ag. The intermetallic compounds (Cu_3Au, AuCu, and Au_3Cu) can decrease the bond strength at higher temperatures (200-325ºC) as a result of Kirkendall voiding. Therefore, these systems are seldom used.

Al-Ni bonds using large diameter aluminium wires, >75mm, are less prone to Kirkendall voiding and galvanic corrosion, thus more reliable than Al-Ag or Al-Au bonds under various environments. This system has been used in high production on power devices and high-temperature applications such as aircraft turbine blades for over fifteen years. In most cases, the nickel is deposited from electroless boride or sulfamate solutions, which results in reliable bonds. However, electroless nickel phosphide solutions that co-deposit more than 6 or 8% of phosphorous can result in both reliability and bondability problems. The main difficulty encountered when bonding to nickel plating is bondability rather than reliability due to nickel surface oxidation. Thus, packages should be bonded soon after they are Ni-plated, protected in an inert atmosphere, or chemically cleaned before bonding. Changing bonding machine schedules, such as impacting the tool-wire-plating with the ultrasonic energy applied, can improve bondability to slightly oxidized nickel surfaces. Various surface preparation techniques (such as sandblasting) are sometimes applied before or after Ni plating to increase bondability.

Copper wire can be bonded to both gold and aluminium substrate. For Cu-Al system, there exist five inter-metallic compounds favouring the copper-rich side. Thus, there is the possibility of various intermetallic failures similar to those of Au-Al system. However, intermetallic growth in Cu-Al bonds is slower than in Au-Al bonds. The intermetallic growth in Cu-Al bonds does not result in Kirkendall voiding bur lowers the shear strength at 150-200ºC due to the growth of a brittle $CuAl_2$ phase. In the temperature range 300-500ºC, bond strength significantly decreases with the increase of the total intermetallic thickness. The rate of Cu-Al intermetallic formation relies on the ambient atmosphere composition. For example, the copper-aluminium bond system is adequately reliable as long as some oxygen is present in the package because Cu oxide prevents or inhibits the growth of void-like grooves under the bond. However, the presence of Cl contamination and water can cause corrosion of the aluminium metallization containing copper-aluminium intermetallics.

Processes

Shortly, wire-bonding process begins by attaching the backside of a chip to a chip carrier. For this purpose, an organic conductive adhesive or a solder (Die Attach) is used. The wires are

then welded using a special bonding tool (capillary or wedge). There are three major bonding processes depending on the bonding agent (heat and ultrasonic energy): thermo-compression bonding (T/C), ultrasonic bonding (U/S), and thermosonic bonding (T/S). Thermo-compression needs high temperature (300-500°C) and pressure, and no ultrasonic energy. The others need ultrasonic energy and low pressure. As for temperature, U/S can be done at room temperature (25°C), while T/S needs 100 – 150°C.

There are two basic forms of wire-bond: ball bond and wedge bond. Currently, thermosonic gold ball bonding is the most widely used bonding technique, primarily because it is faster than ultrasonic aluminium bonding. Once the ball bond is made on the device, the wire may be moved in any direction without stress on the wire, which greatly facilitates automatic wire bonding, as the movement needs to be only in the x and y directions. Using as bonding tool capillary and T/C or T/S as process, ball bond is appropriate for gold wire-bond and aluminium or gold pad finish.

Production speed can reach 10wires/s when T/S is used. Wedge bond needs ultrasonic energy (U/S or T/S processes); the wire-bond can be aluminium or gold, as well as the pad finish. Production speed is lower than ball bond (4wires/s).

Ball bonding (figure 3.1.5). The basic steps of ball bonding are:

- ♦ the formation of the first bond (normally on the chip);
- ♦ the wire loop;
- ♦ the second bond (normally on the substrate).

The wire is passed through a hollow capillary (figure 3.1.5/b), and an electronic-flame-off system (EFO) is used to melt a small portion of the wire extending beneath the capillary. The surface tension of the molten metal from a spherical shape, or ball, as the wire material solidifies. The ball is pressed to the bonding pad on the die with sufficient force to cause plastic deformation and atomic interdiffusion of the wire and the underlying metallization, which ensure the intimate contact between the two metal surfaces and form the first bond (ball bond).

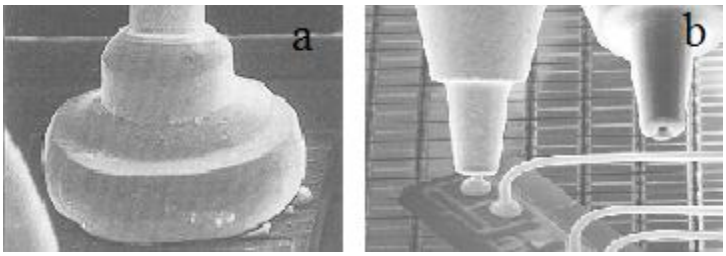


Fig. 3.1.5 a) Ball bond; b) Capillary (after K&S Micro-Swiss)

The capillary is then raised and repositioned over the second bond site on the substrate, a precisely shaped wire connection called a wire loop is thus created as the wire goes.

Deforming the wire against the bonding pad makes the second bond (wedge bond or stitch bond), having a crescent or fishtail shape made by the imprint of the capillary's outer geometry. Then the wire clamp is closed, and the capillary ascends once again, breaking the wire just above the wedge, an exact wire length is left for EFO to form a new ball to begin bonding the next

wire. Ball bonding is generally used in thermo-compression (T/C) or thermosonic bonding (T/S) processes. Heat is generated during the manufacturing process either by a heated capillary feeding the wire or by a heated pedestal on which the assembly is placed or by both depending on the bonding purpose and materials. Ball bonding is generally used in applications where the pad pitch is greater than 100mm, even in applications with pitches of 50mm it has been reported. Gold wire diameter is relatively small (< 75mm) because of its easy deformation under pressure at elevated temperature, its resistance to oxide formation, and its ball formability during a flame-off or electronic discharge cutting process. All the steps of ball bonding are presented in figure 3.1.6.

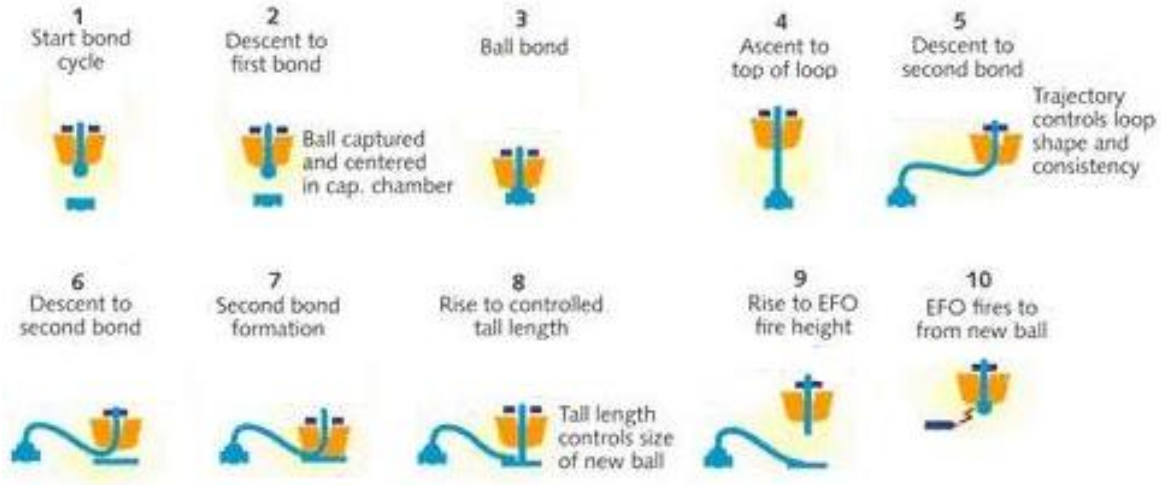


Fig. 3.1.6 Ball bonding steps

Wedge-bonding (figure 3.1.7). The wire is fed at an angle of, usually, 30-60^{o} from the horizontal bonding surface through a hole in the back of a bonding wedge. Normally, forward bonding is preferred, i.e. the first bond is made to the die and the second is made to the substrate. The reason is that it can be far less susceptible to edge shorts between the wire and die. By descending the wedge onto the IC bond pad, the wire is pinned against the pad surface and an U/S or T/S bond is performed. Next, the wedge rises and executes a motion to create a desired loop shape. At the second bond location, the wedge descends making a second bond. During the loop formation, the movement of the axis of the bonding wedge feed hole must be aligned with the centre line of the first bond, so that the wire can be fed freely through the hole in the wedge.
Several methods can be used to end the wire after the second bond. For small wires (< 75mm), clamps can be used to break the wire while machine bonding force is maintained on the second bond (clamp tear), or the clamps remain stationary and the bonding tool raises off the second bond to tear the wire (table tear). The clamp tear process offers a slightly higher yield and reliability than the table tear process due to the force maintained on the second bond during the clamp tear motion. The clamp tear process also offers a light speed advantage over the table tear process due to fewer required table motions. However, the table tear process, with a higher wire feed angle capability and stationary clamp, has the potential to provide slightly more clearance from package obstructions such as a bond shelf or pin grid. For large bonding wires (> 75mm), other methods can be used such as a cutting blade or the placement of the wire into a channel in the wedge for wire termination. As the wedge ascends, the clamped wire is fed under it to begin bonding the next wire.

Wedge bonding technique can be used for both aluminium wire and gold wire bonding applications. The principle difference between the two processes is that the aluminium wire is bonded in an ultrasonic bonding process at room temperature, whereas gold wire wedge bonding is performed through a thermosonic bonding process with heating up to 150^{o}C. A considerable advantage of the wedge bonding is that it can be designed and manufactured to very small dimensions, down to 50mm pitch. However, factors based on machine rotational movements make the overall speed of the process lower than that for thermosonic ball bonding. Aluminium ultrasonic bonding is the most common wedge bonding process because of the low cost and the low working temperature. The main advantage for gold wire wedge bonding is the possibility to avoid the need of hermetic packaging after bonding due to the inert properties of the gold. In addition, a wedge bond will give a smaller footprint than a ball bond, which specially benefits the microwave devices with small pads that require a gold wire junction.

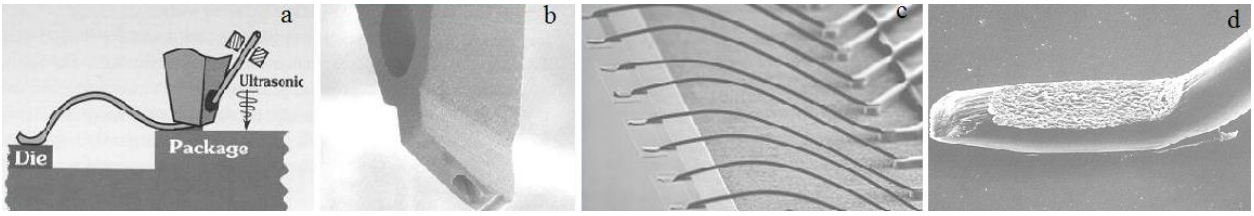


Fig. 3.1.7 Wedge bonding: a) Principle; b) Wedge; c) Connections; d) Wedge bond

Cleaning. A critical condition for a good bondability and reliability of wire-bonding is the bonding surface that must be free of any contaminants. Therefore cleaning is an important work before bonding. The methods, usually adapted, are represented by the molecular cleaning method, plasma or UV-ozone cleaning method.

Plasma cleaning technique employs a high power radio-frequency (RF) source to convert gas used into plasma, the high velocity gas ions bombard the bonding surface and sputter off contaminants from bonding surface by combining the contamination molecules, or physically breaking apart the contamination molecules. In most cases, the ionized gas is oxygen, argon, nitrogen, 80%Ar+20%O_2, or 80%O_2+20%Ar. In addition, O_2/N_2 plasma is also used, which can effectively remove epoxy thermal outgas material from bond pads. The optimum results depend not only upon the gas and RF power, but also upon the fixturing, as well as the specific material being cleaned.

Ultraviolet-ozone cleaning technique employs an UV-ozone cleaner designed to emit significant amounts of radiation of 1849Å and 2537Å wavelengths. The cleaning process consists in the following reactions:

♦ the 1849Å UV energy breaks up the O_2 molecule into atomic oxygen (O+O) which combines with other O_2 molecules to form ozone, O_3;

♦ the ozone breaks up again into atomic oxygen and O_2 with 2537Å UV. Any water present may also be broken into the OH- free radical;

♦ all of these (OH, O_3, and O) can react with hydrocarbon to form CO_2 + H_2O which leave the bonding surface as a gas;

♦ the strong 2537Å UV may additionally break the chemical bonds of the hydrocarbon, accelerating the oxidation process.

Although both UV-ozone and plasma cleaning method can be used to remove organic contamination from bonding pads, their effectiveness is strongly dependent on the specific contaminant. For example, bondability of the thick-film gold cannot be improved by oxygen plasma, possibly due to the oxidation of the bonded elements, such as copper. The best results are obtained with oxygen free argon plasma or solvent cleaning method. In addition, some contaminants, such as Cl- and F- may not be removed by any of these cleaning methods because they can become chemically bound. Thus, various solvent techniques including solution, vapour-phase fluorocarbons, ionographic, and DI water, in some cases, are used.

Some wire-bonding equipment is shown in figure 3.1.8.

Bonding parameters are very important because they control the bonding yield and reliability directly. The key variables for wire-bonding are:

- ♦ bonding force and pressure uniformity;
- ♦ bonding temperature;
- ♦ bonding time;
- ♦ ultrasonic frequency and power.

The optimum conditions are controlled by wire type, pad metallization, and device configurations. Therefore, for every kind of product, a serious of bonding tests has to be performed by varying bonding parameters to draw out the optimum bonding conditions.

Evaluation of bond pull strength is used to help the definition. In the evaluation, three sets of curves of bond pull strength versus power, time, or clamping force can be obtained by varying one of these parameters while holding the other two constant at their optimum.

Fig. 3.1.8 Wire-bonding equipments

Each curve is similar to, and can be related to, the curve of bond pull strength versus wire deformed width. As each parameter is increased, the bond grows stronger in lift off strength. At the same time, due to wire deformation, the transition from the wire into the bond becomes weaker. The failure mode changes from bond failure (lift off) to wire breakage failure. The wire-bond can be evaluated with visual method and mechanical testing, depending on the requirements and the situation that may arise from previous experiences with a particular package or mechanical techniques. Visual method uses optical microscope, scanning electron microscope (SEM), and other analytical instruments to find the undesired bonds. Mechanical testing is employed for the evaluation of bond strength.

Applications

Stack dice. Wire-bonding is the primary method of making interconnections within an integrated circuit (IC) between each of the I/O pads on the silicon chip and its associated pin during semiconductor device fabrication. The chip is attached to the substrate with the bonding pads facing away from the substrate. Connecting wire-bonds made of gold or aluminium are then attached by welding on the chip pads, pulled to the substrate pads and again attached by welding.

Advantages:

- ♦ Well proven method with good yield;
- ♦ Low cost for low to medium production volumes;
- ♦ No special chip metallization required, chips are normally designed for wire bond;
- ♦ Can also be used if a few extra crossovers are needed on the substrate;
- ♦ Function well down to a pad-pitch of approximately 80mm.

Disadvantages:

- ♦ Relatively slow (one bond at a time);
- ♦ The size and movement of the bond-head may restrict how closely chips can be placed;
- ♦ Inductance of bond wires may limit the use in extreme high frequency devices;
- ♦ Bondable (pure) gold is normally required on the substrate.

A major goal of the development of advanced packaging technology is to reduce the size, weight, and power consumption of electronics components using state-of-the-art commercial technologies. One of the novel concepts involves the 3D approach when designing and producing new systems. Techniques such as die and package stacking naturally contribute to a reduction of the spatial footprint of any given electronic system design. Interconnections between the different components of the stack can be done by wire-bonding (figure 3.1.9). While standard wire-bonding might have a loop height of 150 to 175µm, die stacking could require loop heights under 100µm. Today, 125µm loop with 25µm wire is achievable. One way to achieve even lower loop heights is to use reverse bonding as shown in the Intel quad stack photo (figure 3.1.10). This technique puts the ball bond on the substrate, and then the stitch bond is made to the die pads. If there is concern about damaging the die glassivation with the bonding tool, a stud bump can be bonded to the die prior to the reverse bonding, and the stitch bond can be made to the stud bump.

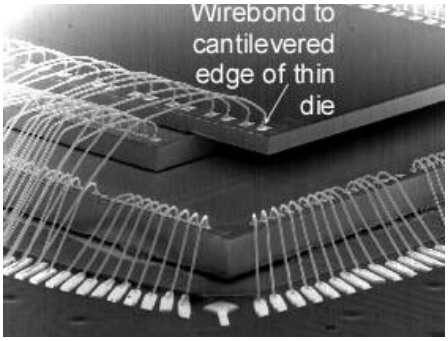


Fig. 3.1.9 Intel 3-die stack

In many cases, die stacking results in a structure that requires the die interconnection wire bonds to be physically crossed. Hence, electrical shorting of the routing interconnections between stacked dies can become a problem. A solution to this problem is the introduction of an interposer into the stack. The interposer is an intermediate layer with a higher circuit density that reroutes the connections of a die to allow wire-bonding to another die or package without the need to cross the connections (figure 3.1.11). Using wire-bonding, SanDisk reported the built of nine-stacks of 30µm-thick dice. If required, speed, performance and density can be achieved by interconnecting bond pads with wire bond.

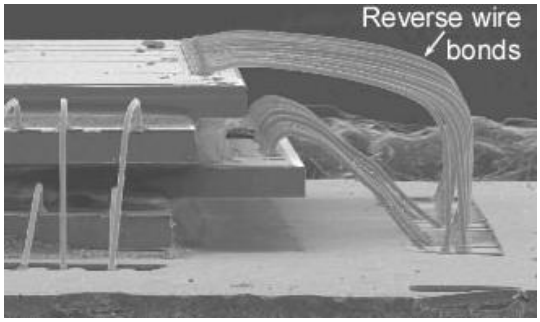


Fig. 3.1.10 Intel quad stack

Radio Frequency Integrated Circuit (RFIC). The wireless industry is undergoing tremendous growth, spurred in part by small, low-cost Radio Frequency Integrated Circuits. The simplest RFICs are designed to perform a single, discrete function, such as amplification or mixing.

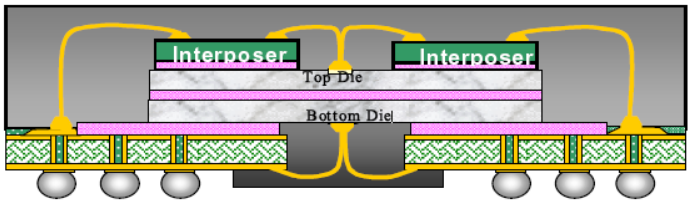


Fig. 3.1.11 A stack package structure with interposers

These chips are usually less than one square millimetre in area, and require fewer than a dozen connections to off-chip circuitry. More involved RFICs can contain complete receive

and/or transmit chains into the total RF portion of a radio. These transceiver chips require several dozen high-frequency I/O connections to the printed circuit board (PCB).

The performance of a radio frequency integrated circuit can be dramatically affected by the package environment. The ideal package creates a transparent link between the printed circuit board signals and the silicon chip. Any deviation from the ideal package causes the input signal to be degraded. This degradation manifests itself in three ways: excessive Insertion Loss (IL), insufficient Return Loss (RL), and pin-to-pin isolation.

Plastic package technology has been the standard of the integrated circuit industry for many years, and this will continue for the foreseeable future. This is due primarily to the low-cost and relatively high performance of the technology. Higher performance ceramic leaded packages have been developed for high performance applications, but traditional ceramic packages are significantly more expensive than plastic approaches. One crucial aspect of the use of these packages is obtaining an accurate equivalent circuit model, for use in the overall IC design process. Figure 3.1.12 is the cross section of a SO-type plastic leaded package. Included in the diagram is the outline of the plastic body, lead frame, bond wire, and die.

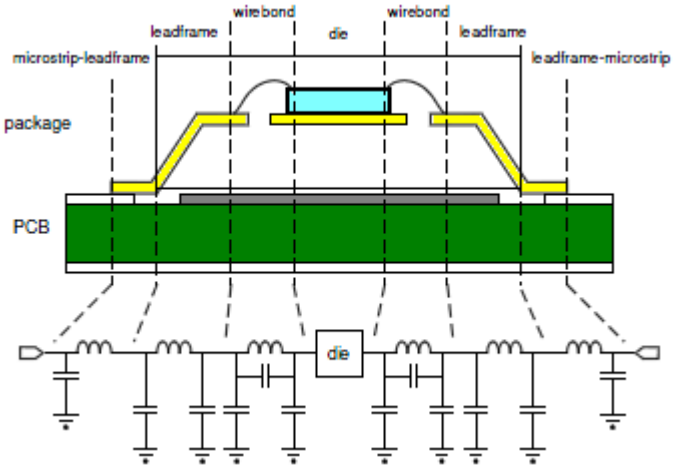


Fig. 3.1.12 Traditional SO-type leaded package: Cross-section showing the origination of package parasitics

Due to its robustness, inexpensive costs and capability to tolerate die thermal expansion, wire-bonding continue to be the dominant technique to connect an RFIC to the package. However, their inductance creates significant challenges for RFIC design, as well as some unique opportunities. The wire bond inductance is dependent on the length of the bond wire and the cross sectional area. Most bond wires are 25-30µm in diameter and between one and two millimetres in length. An approximate formula that has proven accurate at low frequencies is given by F.W. Grover (Inductance Calculations: Working Formulas and Tables):

$$L\ [\mu H] = 0.002\ l\ \{\ln(2l/r) - 0.75\}$$

where l and r are the length and radius of the bond wire in [cm] respectively.

More accurate models of bond-wire inductance require full 3D simulations, and account for the curvature of the wire bond, as well as the height above the ground plane. Values of approximately 1nH/mm are commonly used as a ‘rule of thumb’, but more accurate results are often required. In addition, the effect of paralleling two bond wires must be taken into account, in this case experiments proved that the equivalent series inductance drops by approximate 30 percent when two bond wires are in parallel. In order to accurately model the inductance to very high frequencies, a second-order coefficient of inductance had to be added to account for the decreasing inductance at higher frequencies.

3.1.2 Tape Automated Bonding (TAB)

Basics

Tape Automated Bonding (TAB), is a process of mounting a die on a flexible tape made of polymer material, such as polyimide (figure 3.1.13). The mounting is done such that the bonding sites of the die, usually in the form of bumps or balls made of gold or solder, are connected to fine conductors on the tape, which provide the means of connecting the die to the package or directly to external circuits. Sometimes the tape on which the die is bonded already contains the actual application circuit of the die. The film is moved to the target location, and the leads are cut and soldered as necessary. The bare chip may then be encapsulated ("glob topped") with epoxy or plastic. Compared to a Chip-on-Board assembly, where chips are directly wire-bonded to the PCB, TAB has the advantage of reduced pad sizes.

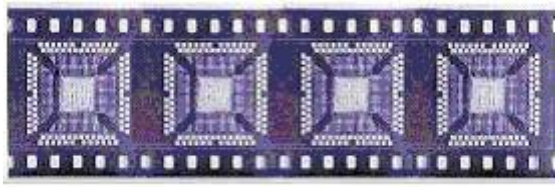


Fig. 3.1.13 Example of TAB devices

TAB offers the following advantages:

- ♦ it allows the use of smaller bond pads and finer bonding pitch;
- ♦ it allows the use of bond pads all over the die, not just on the die periphery, and therefore increases the possible I/O count of a given die size;
- ♦ it reduces the quantity of gold needed for bonding;
- ♦ it limits variations in bonding geometry;
- ♦ it has a shorter production cycle time;
- ♦ it results in better electrical performance (reduced noise and higher frequency);
- ♦ it allows the circuit to be physically flexible;
- ♦ it facilitates multi-chip module manufacturing.

The disadvantages of TAB are as follows:

- ♦ time and cost of fabricating the tape;
- ♦ the need to 'tailor-fit' the tape pattern after each die;
- ♦ capital expense for TAB equipment since TAB manufacturing requires a set of machines different from those used by conventional processes.

Historically, TAB was invented by Frances Hugle in Silicon Valley and commercialized in 1966 by General Electric Research Laboratories, who used it with small-scale integration (SSI) devices. The term 'Tape Automated Bonding' was coined by Gerard Dehaine of Honeywell Bull in 1971. TAB was created as a low cost alternative to wire-bonding. Through the 1970s, TAB received strong consideration and attention but experienced relatively little industry acceptance, except in Japan and Taiwan. Japan had the largest number of companies to commercialize TAB. TAB saw its most widespread adoption in the 1980s as surface mount technology exploded. With its ability to handle high-density I/O and high speed circuitry of very-large-scale-integration (VLSI), TAB has been applied to a variety of consumer, medical, security, computer, peripheral, and telecommunication, automotive and aerospace products.

Materials

The TAB bonds connecting the die and the tape are known as inner lead bonds (ILB), while those that connect the tape to the package or to external circuits are known as outer lead bonds (OLB).

OLBs are of copper with a final metallisation of tin or gold, and the pads to which they are bonded are normally coated with eutectic tin-lead solder. The mechanical stability and thermal cycling behaviour of the outer lead bond are determined by the ductility of the copper lead and the geometry of the solder joint formed during the OLB process. Whilst sufficient solder is needed, the solder thickness must be reduced in fine pitch applications in order to avoid solder bridges.

The tape used in TAB is usually single-sided, although two-metal tapes are also available. Copper, a commonly-used metal in tapes, can be electrodeposited on the tape or simply attached to the tape using adhesives. The metal patterns of the circuit are imaged onto the tape by photolithography.

Standard sizes for polyimide tapes include widths of 35mm, 45mm, and 70mm and thicknesses between 50 to 100 microns. Since the tape is in the form of a roll, the length of the circuit is measured in terms of sprocket pitches, with each sprocket pitch measuring about 4.75mm. Thus, a circuit size of 16 pitches is about 76mm long.

Polyimide is a polymer of imide monomers. There are two general types of polyimides. One type, so-called linear polyimides, is made by combining imides into long chains. Aromatic heterocyclic polyimides are the other usual kind, where R' and R" are two carbon atoms of an aromatic ring. Examples of polyimide films include Apical, Kapton, UPILEX, VTEC PI, Norton TH and Kaptrex. Thermosetting polyimides are known for thermal stability, good chemical resistance, excellent mechanical properties Therefore, they are used in the electronics and semiconductor industries.

There are three generic constructions used in common TAB tapes:

- ♦ All-metal tape, which is a single layer of copper without a dielectric layer;
- ♦ Gold plated copper tape (as used by NEC for the SX3 super computer);
- ♦ Two-layer tape, where copper is directly laminated to polyimide;

♦ Three-layer tape, with copper and polyimide but a separate adhesive layer.

Processes

The first process used etched copper tape laminated to a sprocketed 35mm polyimide film (figure 3.1.14) and an automated reel-to-reel assembly system (figure 3.1.15). To facilitate the connection of the die bumps or balls to their corresponding leads on the TAB circuit, holes are punched on the tape where the die bumps will be positioned. The conductor traces of the tape are then cantilevered over the punched holes to meet the bumps of the die. The inner section of the copper tape was attached by thermo-compression bonding to gold bumps on the die pads, and the outer section soldered or welded to the board.

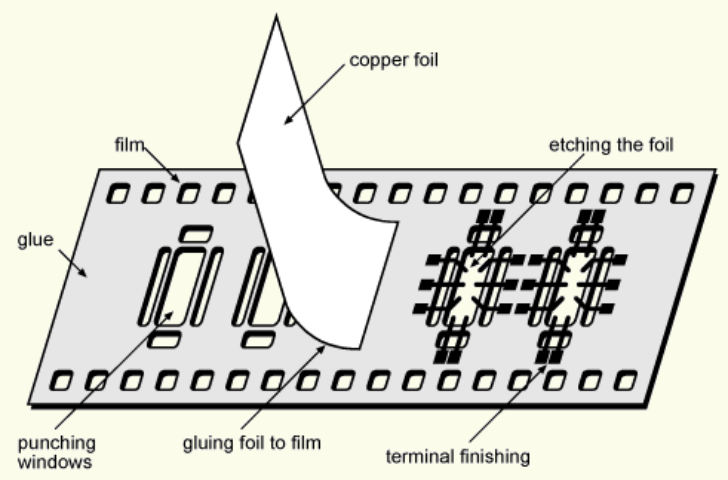


Fig. 3.1.14 Progressive build-up of a TAB tape

There are two common methods of achieving a bond between the gold bump of the die and the lead of a TAB circuit:

♦ single-point thermosonic bonding;
♦ gang or thermo-compression bonding.

Single-point bonding (figure 3.1.16), as the name implies, connects each of the die's bond site individually to its corresponding lead on the tape. Heat, time, force, and ultrasonic energy are applied to the TAB lead, which is positioned directly over the gold bump, forming inter-metallic connections between them in the process. For the thermosonic bonding used in the single point TAB technology, the deformation behaviour of the bonding material and the working of the ultrasonic vibration are very significant. An applied load that is one of the bonding parameters in the single point TAB process has influence on the deformation behaviour and the working of the ultrasonic vibration. Single-point bonding is a more time-consuming process than gang bonding.

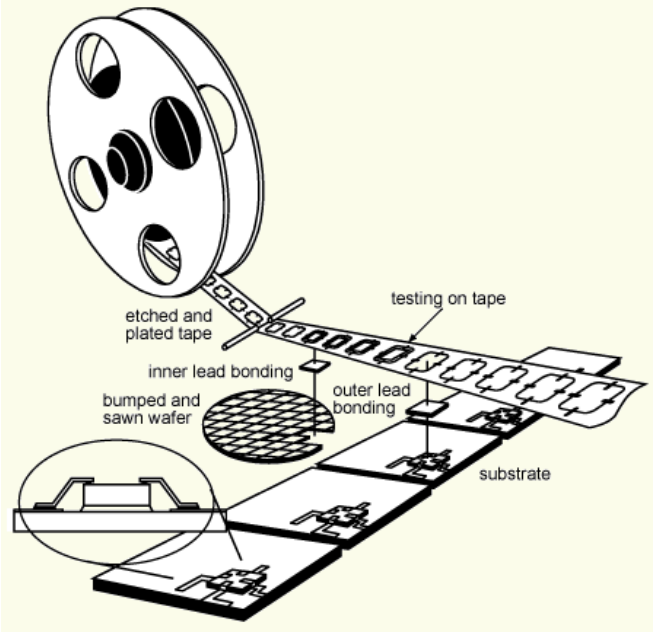


Fig. 3.1.15 Schematic of a Farco ‘bumped’ wafer TAB processing machine

Gang bonding. The original TAB inner lead bonding process was thermo-compression gang bonding. It employs a specially designed bonding tool to apply force, temperature, and time to create diffusion bonds between the leads and bumps, all at the same time. This, however, may cause cracks in the chip passivation and sometimes one and one lead is connected at the time to allow better control of the bonding. Without the use of ultrasonic energy, this type of bonding is simply referred to as 'thermo-compression' bonding.

Gang bonding offers a high throughput rate, and is therefore preferred to single-point bonding. After gang bonding, the die, bonds, tape leads, and part of the tape are covered with an encapsulant, which provides mechanical and chemical protection to the circuit after its curing. The die is then electrically tested, after which the useable part of the tape is punched from the frame for assembly into the final application.

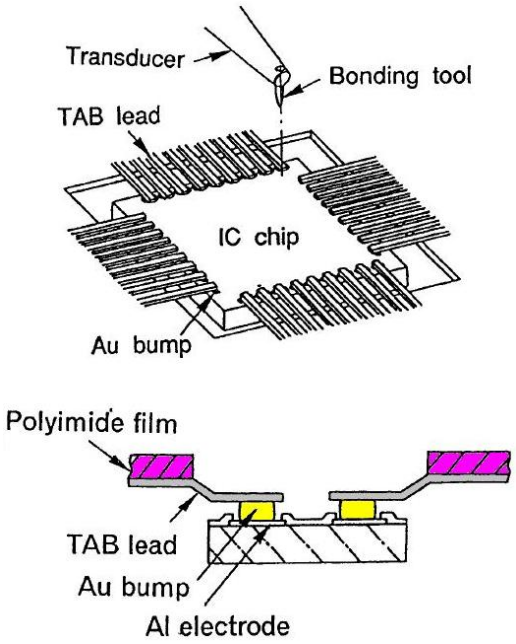


Fig. 3.1.16 Single point TAB

Examples of TAB equipment are shown in figure 3.1.17. In the assembly plant, the tape is cut in such way that the outer part of the conductors (leads) is exposed. The chip/film assembly is then aligned and soldered or glued to the substrate using conductive adhesive. Normally the cutting and bonding is done in one operation with a tool specially designed for the chip/film assembly. In some applications, a technique called "flip-TAB" is used. In this case, the chips are faced towards the substrate before bonding. This allows much shorter wires and therefore increased high-frequency properties as well as increased packaging density.

The main steps of a TAB process are:

- ♦ The flexible polyimide tape is perforated along the edges and two windows are opened in the middle for the chip and the leads;
- ♦ Copper foil is stuck onto the tape;
- ♦ Floating leads, protruding into the inner window are etched from the copper foil by using photolitography;
- ♦ A flip chip is mounted onto tape.

Thus, TAB is a better alternative to conventional wire-bonding if very fine bond pitch, reduced die size, and higher chip density are desired. It is also the technique of choice when dealing with circuits that need to be flexible, such as those that experience motion while in operation, e.g., printers, automotive applications, folding gadgets, etc. TAB is generally more cost-effective for use in high-volume production, since returns on the time and cost of developing the tape will be maximized under this situation. Its principal use is as driver connections on LCD panels (figure 3.1.18).

Fig. 3.1.17 Examples of TAB equipment

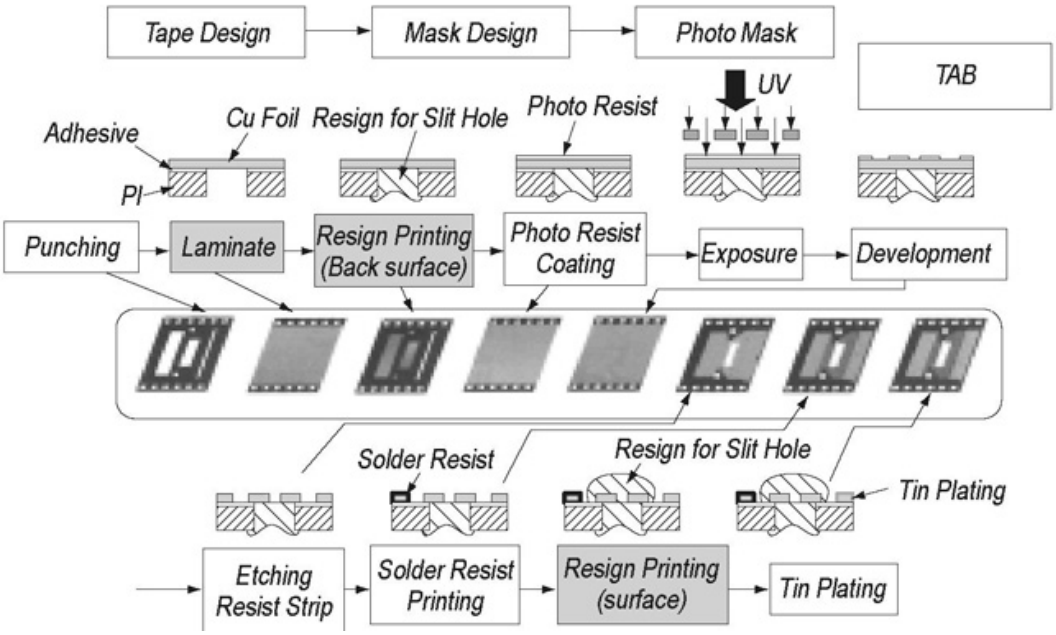


Fig. 3.1.18 The TAB manufacturing process for LCD

Applications

Still increasing clock frequencies call for minimum parasitic capacities and inductances. TAB allows bigger cross-sections for the connections and therefore reduced parasitic effects. In addition, the bigger cross-sections enhance the heat flow from the IC and contribute to achieve higher power densities. Additional heat sinks can be mounted on the free IC back. 'Ground plane' tape has one or more extra metal planes to provide controlled impedance (figure 3.1.19). This considerably improves cross-talk and switching noise with terminated systems, but is not so effective for circuits with high input impedance drivers, such as most CMOS applications. These advantages were used for example from Intel for mounting the Pentium processors. An important factor for the shrink of systems is the ratio between active and passive footprint. The approach at the ideal ratio 1 is accomplished by the Flip-Chip technology, but also COB and Chip Scale Packages contribute to the miniaturisation.

TAB may add another advantage by combining other components with the IC on the flexible tape or eliminating additional substrates, for example by gluing the Tape directly onto a LCD or sensor. These properties allow TAB to be considered as an interesting interconnection alternative: TQFP (Tape Quad Flat Pack) and TBGA (Tape Ball Grid Arrays) are novel packages using TAB as a basic interconnect. Microprocessors and ASIC's benefit from TAB in the fields where high frequencies, high pin counts or high power dissipation are concerned. Optical Encoders need a minimum distance between the optical system and the chip surface. The very robust TAB interconnection, the flat profile and the hermetic sealing give TAB many advantages. Miniaturized systems, as Hearing aids, are easily realised with TAB, taking benefit from the combination of elements on a flexible substrate and the possibility of 3-dimensional mountings.

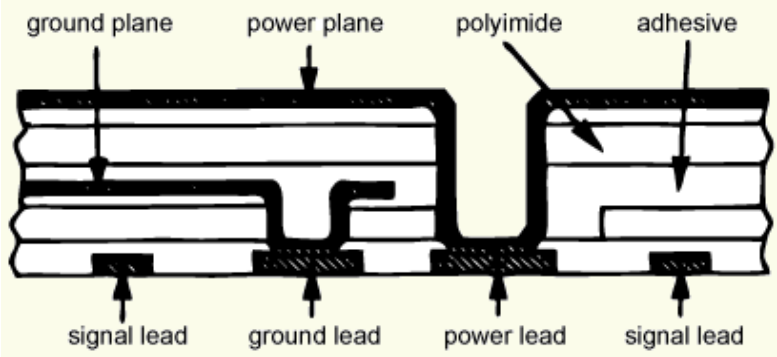


Fig. 3.1.19 Schematic cross-section of three-level TAB tape

LCD Drivers are probably best suited for TAB, combining all the assets needed:

- ♦ Flat profile (Chip thickness plus 60mm);
- ♦ High pin-count (180 - 250 I/O);
- ♦ Lowest pad pitch (actually down to 60mm);
- ♦ Automatic assembly (very high quantities);
- ♦ Flexible substrate (direct attach to the LCD).

Summarising the pros and cons of TAB:
Advantages:

- ♦ Well suited for very high volume production; all bonds in one operation and the chips is delivered on rolls or in cartridges;
- ♦ Good electrical performance especially if a tape with a separate ground plane is used;
- ♦ Fan-out on the tape makes it possible to mount chips with fine pad pitch on a substrate with a much larger pad pitch.

Disadvantages:

- ♦ Different bonding tools must be used for different outer lead area dimensions;
- ♦ Bonding tools are expensive;
- ♦ TAB film must be specially designed for every chip type;
- ♦ Normally the chips need special bumping and metallurgy, which prohibit the use of off the shelf chips;
- ♦ Cross-talk may occur in single layer film at high frequency, especially if the length of the conductors on the film is large;

♦ Inductance of long conductors on single layer films may cause problems in the power supply of power hungry chips.

3.1.3 Flip Chip (FC)

Basics

The concept of flip-chip process where the semiconductor chip is assembled face down onto circuit board is ideal for size considerations, because there is no extra area needed for contacting on the sides of the component. In high frequency applications where length of the connection path is important flip-chip process is superior to other interconnection methods. In flip-chip joining there is only one level of connections between the chip and the circuit board. Hence, reliability is better than with packaged components due to decreased number of connections. Flip chip components are predominantly semiconductor devices; however, components such as passive filters, detector arrays, and MEMS devices are also beginning to be used in flip-chip form. The technology has been driven by IBM for mainframe computer applications since the end of 60`s. Today flip-chips are widely used for watches, mobile phones, portable communicators, disk drives, hearing aids, LCD displays, automotive engine controllers as well as the main frame computers.

A brief history of flip-chip technology is presented below:

1961: IBM invented Solid Logic Technology (SLC);

1964: IBM launched in production Solid Logic Technology (System 360);

1965: IBM introduced Controlled Collapse Chip Connection (C4) process;

1988: Hitachi provided underfills to IBM that consistently improved thermal cycling and sealed out moisture;

Late 80’s – early 90’s: Motorola became a low-cost, high volume "polymer circuit" company;

Early 90’s: Alpha Metal's polymer group, Advanced Products Division, decided to tackle the "underfill bottleneck" problem: their first underfill product dropped the cure time down to 30 minutes, with much faster flow.

Flip chip, also known as Controlled Collapse Chip Connection (hence its acronym, C4) or Direct Chip Attach, DCA (since the chip is directly attached to the substrate, board, or carrier by the conductive bumps), is a method for interconnecting a device to external circuitry with solder bumps that have been deposited onto the chip pads. The solder bumps are deposited on the chip pads on the top side of the wafer during the final wafer processing step. In order to mount the chip to external circuitry (e.g., a circuit board or another chip or wafer), it is flipped over so that its top side faces down, and aligned so that its pads align with matching pads on the external circuit, and then the solder is flowed to complete the interconnect. This is in contrast to wire bonding, in which the chip is mounted upright and wires are used to interconnect the chip pads to external circuitry. Summarising, the process steps are:

♦ Integrated circuits are created on the wafer;

♦ Pads are metalized on the surface of the chips;

♦ Solder dots are deposited on each of the pads;

- ♦ Chips are cut;
- ♦ Chips are flipped and positioned so that the solder balls are facing the connectors on the external circuitry;
- ♦ Solder balls are then remelted (typically using hot air reflow);
- ♦ Mounted chip is “underfilled” using an electrically-insulating adhesive.

Potentially flip chip technology is cheaper than wire bonding because bonding of all connections takes place simultaneously whereas with wire bonding one bond is made at a time.

The advantages of flip-chip are:

- ♦ Smaller size: smaller IC footprint (only about 5% of that of packaged IC e.g. quad flat pack), reduced height and weight;
- ♦ Increased functionality: the use of flip chips allow an increase in the number of I/O. I/O is not limited to the perimeter of the chip as in wire bonding. An area array pad layout enables more signal, power and ground connections in less space. A flip chip can easily handle more than 400 pads;
- ♦ Improved performance: short interconnect delivers low inductance, resistance and capacitance, small electrical delays, good high frequency characteristics, thermal path from the back side of the die;
- ♦ Improved reliability: epoxy underfill in large chips ensures high reliability. Flip-chips can reduce the number connections per pin from three to one;
- ♦ Improved thermal capabilities: because flip chips are not encapsulated, the back side of the chip can be used for efficient cooling;
- ♦ Low cost: batch bumping process, cost of bumping decreases, cost reductions in the underfill-process.
- ♦ Noiseless. Generally there are good reasons to assume that solder joints used in flip-chip joining do not generate harmful noise. In digital CMOS processor designs the power supply noise is determined by the core and input drivers and by their ability to draw instantaneous current from the supply and on the way how the on-chip power distribution structures interact with the package and board design. As reported by H. Hashemi and D. Herrell [“Power Distribution Fidelity of Wire-bond Compared to Flip Chip Devices in Grid Array Packages"] the flip chip connections, when compared to the wire bonded design, improve the power disturb performance by at best a factor of two. This is because the on-chip and on-package power grid distribution inductance can dominate the low inductance of the flip chip connections. They found that on-chip decoupling capacitors in conjunction with a substantial on-chip power grid structure can provide a much lower noise environment for both wire bonded as well as flip chip connected devices.
- ♦ The flip chip assembly is ideal for high frequency applications because of the very short current path between the component and the substrate. For solder joined flip chip connections the joints are metallurgical joints with series resistance of the order of 1mΩ. The series inductance is very much smaller than that of wire bonded joint or leaded package. For typical leaded package the series inductance is from 5 to 10nH while that for flip chip solder joint is only about 0.025nH. Because of the smaller capacitance, smaller inductance and smaller resistance of the flip chip joints compared

with wire bonded joints the propagation delay is also considerably smaller in the flip chip structure.

Disadvantages of flip-chip are:

- ♦ Difficult testing of bare dies;
- ♦ Limited availability of bumped chips;
- ♦ Challenge for PCB technology as pitches become very fine and bump counts are high;
- ♦ For inspection of hidden joints an X-ray equipment is needed;
- ♦ Weak process compatibility with SMT;
- ♦ Handling of bare chips is difficult;
- ♦ High assembly accuracy needed;
- ♦With present day materials underfilling process with a considerable curing time is needed;
- ♦ Low reliability for some substrates;
- ♦ Repairing is difficult or impossible.

Although flip chip technology has been used already for about 30 years, it is still in quite limited use. It has many technical variations which have very different levels of maturity and fairly restricted availability. The flip chip technology using solder joining is already in a fairly mature state. The limitations are at least partly related to the limited availability of bumped components and limited compatibility with available SMD processing equipment.

A schematic of a typical flip-chip mounting is presented in figure 4.1.18.

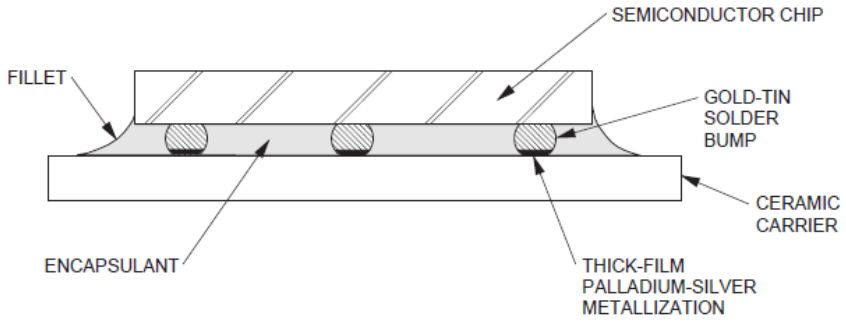


Fig. 3.1.20 A typical flip-chip mounting

Materials

Referring to flip-chip technology it had to be considered two main elements: the bump and the under bump metallisation (UBM).

The preferred bump material for thermo-compression flip chip bonding is gold. These bumps can made using the conventional electrolytic gold plating (used for TAB bumps) or the stud bumping method. The gold ball bumps (figure 3.1.21) are fabricated with a flexible low cost bumping technique based on the conventional wire bonding procedure. Established wire bonding machines can be used; therefore, expensive bumping process equipment for sputtering lithography and plating is not necessary. The gold wire must be alloyed with 1% Pd to ease the

breaking of wire above the bump. During bump formation the wafer/substrate must be heated to 150 - 200ºC.

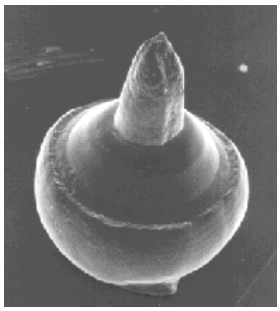


Fig. 3.1.21 Gold ball bump

The final metal layer of most IC bond pads is aluminium, providing a satisfactory surface for conventional wire bonding, but an improper surface to most conductive bumps. Aluminium forms an oxide immediately upon exposure to air, and this native oxide is an electrical insulator. A wire bond in its formation scrubs through the insulating oxide to weld with the underlying metal. Aluminium is not a readily solderable surface, neither wettable nor bondable by most solders. Aluminium may corrode over time when not protected from the environment. Consequently, successful bumping must first replace the oxidized aluminium surface with a more hospitable material, the UBM.

This material must meet several requirements:

- it must provide a strong, stable, low resistance electrical connection to the aluminium;
- it must adhere well both to the underlying aluminium and to the surrounding IC passivation layer, hermetically sealing the aluminium from the environment;
- it must provide a strong barrier to prevent the diffusion of other bump metals into the IC;
- it must be readily wettable by the bump metals, for solder reflow.

UBM usually consists of a multilayer metal stack. Processes used for layers deposition are:

- sputtering: a vacuum based technology, the most reliable and flexible process
- electroless Ni(P)Au: does not require vacuum or photolithographic processing; it is used for inexpensive an low I/O count die (IC for smart card).

The most common adhesion/barrier layers today are Ti and TiW (10%/90% wt).

Interconnection of the bump to the substrate metallization is achieved using a bond material providing both an electrical and mechanical interface between the bump and substrate trace. Often the bump and bond materials are the same, or the bond and encapsulant materials are the same. That is to say, the function of the bump and the bond or the bond and the encapsulant, is accomplished using a single material solution such as eutectic lead-tin or lead-free solder or anisotropic conductive adhesives, respectively.

Processes

There are many different alternative processes used for flip-chip joining:

♦ Flip chip process by solder joining: In flip chip soldering process solder bumped chips are soldered onto the circuit board. Solder is usually, but not always, deposited also on to the substrate pad areas. For fine pitch applications, solder can be deposited e.g. by electroplating, solder ink jet or solid solder deposition. Tacky flux is applied to the solder contact areas either by dipping the chip into a flux reservoir or by dispensing flux onto the substrate. For coarse pitch applications (>0.4mm) solder paste is deposited on the substrate by stencil printing. The bumps of chips are placed into the tacky paste and they are reflowed in an oven. After the reflow process cleaning of the flux is preferred. The underfill material is applied by dispensing along one or two sides of the chip, from where the low viscosity epoxy is drawn by capillary forces into the space between the chip and substrate. Finally the underfill is cured by heat. Repairing of the flip chip joint is usually impossible after the underfill process. Therefore testing must be done after reflow and before the underfill application.

♦ Flip chip joining by thermo-compression (figure 3.1.22): In the thermo-compression bonding process, the bumps of the chip are bonded to the pads on the substrate by force and heat applied from an end effector. The process requires gold bumps on the chip or the substrate and a correspondingly bondable surface (e.g. gold, aluminium). The bonding temperature is usually high, e.g. 300ºC for gold bonding, to soften the material and increase the diffusion bonding process. The bonding force can be up to 1 N for an 80mm diameter bump. Due to the required high bonding force and temperature, the process is limited to rigid substrates such as alumina or silicon. Additionally, the substrates must have a high planarity. A bonder with high accuracy in the parallelism alignment is required. In order to avoid pre-damaging of the semiconductor material, the bonding force must be applied with a gradient.

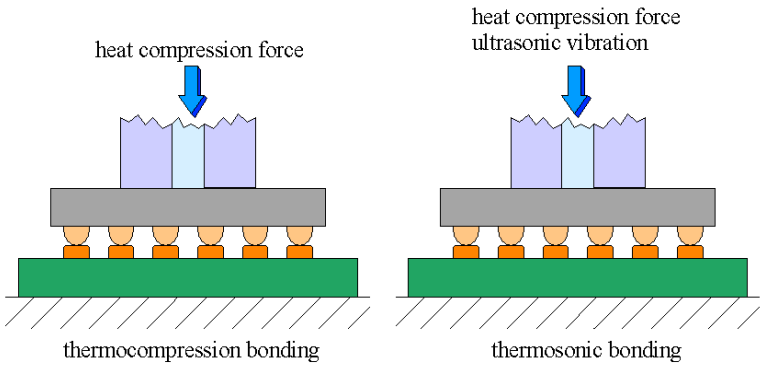


Fig. 3.1.22 Flip chip joining by thermo-compression

♦ Flip chip thermo-sonic joining: The thermo-compression bonding process can be made more efficient by using ultrasonic power to speed up the welding process. Ultrasonic energy is transferred to the bonding area from the pick-up tool through the back surface of the chip. The thermo-sonic bonding introduces ultrasonic energy that softens the bonding material and makes it vulnerable to plastic deformation. The main benefit of the method compared to thermo-compression is lower bonding temperature and shorter processing time. One potential problem associated with thermosonic bonding is silicon cratering. It is generally believed that such damage results from excessive ultrasonic vibration.

♦ Flip chip joining using adhesives (figure 3.1.23): Conductive adhesives have become a viable alternative to tin-lead solders also in flip chip joining. Adhesively bonded flip chip combines the advantages of thin structures and cost efficiency. The advantages of conductive

adhesives include ease of processing, low curing temperatures, and elimination of the need to clean after the bonding process. Anisotropically conductive adhesives have also the ability to connect fine pitch devices. Figure 3.1.22 shows a schematic drawing of flip chip bonding with isotropically and anisotropically conductive adhesives (ICAs and ACAs).

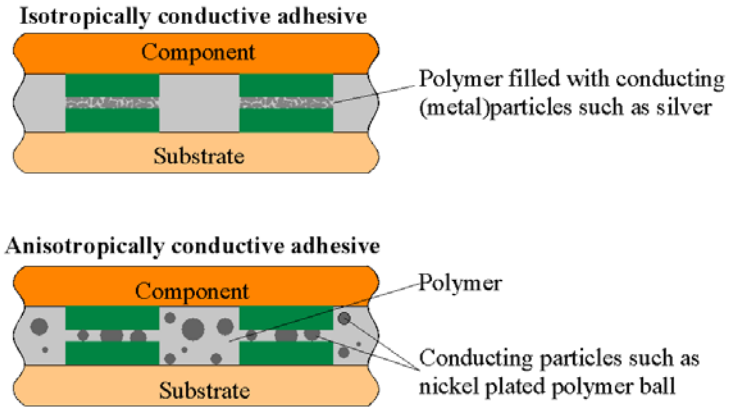


Fig. 3.1.23 Flip-chip joining by conductive adhesive

Also non-conductive adhesives can be used for flip chip bonding, in this case the joint surfaces are forced into intimate contact by the adhesive between the component and substrate. Isotropically conductive adhesives are pastes of polymer resin that are filled with conducting particles to a content that assures conductivity in all directions. Generally, the polymer resin is epoxy and conducting particles are silver. Anisotropically conductive adhesives are pastes or films of thermoplastics or b-stage epoxies. They are filled with metal particles or metal coated polymer spheres to a content that assures electrical insulation in all directions before bonding. After bonding, the adhesive becomes electrically conductive in z-direction. The metal particles are typically nickel or gold and these metals are also used to coat polymer spheres.

Maximum recommended junction temperature is 140^{o}C without underfill and 150^{o}C with underfill. The thermal resistance for one joint is 1000 - 1500^{o}C/W. The thermal resistance from chip to substrate through the flip chip joints may be roughly obtained by dividing the thermal resistance of one bump by the number of bumps in the chip. This is the worst case situation because there are also other routes of heat flow which may affect the cooling of the chip. Extra dummy bumps increase the cooling efficiency. High thermal conductivity underfills can be used. When efficient cooling is needed, like in high power processor packages, back side of the chip can be used for thermal management of the package.

Production issues

For production of circuit boards with solder bumped flip chips the main steps of process are:

- ♦ die bumping;
- ♦ loading of chips and substrates;
- ♦ pick-up the chip;
- ♦ flux or solder application;
- ♦ alignment of chip;
- ♦ chip placement;

- ♦ reflow;
- ♦ underfill-application;
- ♦ underfill-curing.

The assembly of flip chip components needs some special tools compared with normal SMD mounting.

Fig. 3.1.24 Flip-chip assembly line containing a separate flux dispensing unit (Asymtek)

The modifications needed are chip handling including flipping the die in the chip loading unit, dispenser flux application or alternatively an extra dipping step and flux reservoir. Underfill-dispensing and curing equipment are also needed. The conventional underfill process is based on flow of underfill material driven capillary forces under the chip. This needs time of several minutes. New more rapid underfill processes and new materials are under development. Figure 3.1.24 presents a Flip-chip assembly line. The accuracy needed in alignment is dependent on the pitch used. Also the self alignment behaviour of solder material lowers the accuracy requirement. For reflow soldering conventional reflow ovens used in SMD process can be used.

Laser soldering is often applied as selective laser soldering. Parts, which can`t be soldered by wave or reflow soldering, are soldered subsequently by lasers. This can be parts, which are heat sensitive or need a special temperature program due to their part size. The diagram below (figure 3.1.25) shows a process, which can be defined by a simple programming language and stored in the Laser soldering machine program.

The green curve in the diagram shows the progress of the set point temperature. The red curve represents the real, controlled temperature in the laser’s focus (actual temperature). The black curve denotes to the controller output signal for the diode laser with analog voltage. The black curve corresponds with the 0-100% of the axis scale on the right side of the diagram.

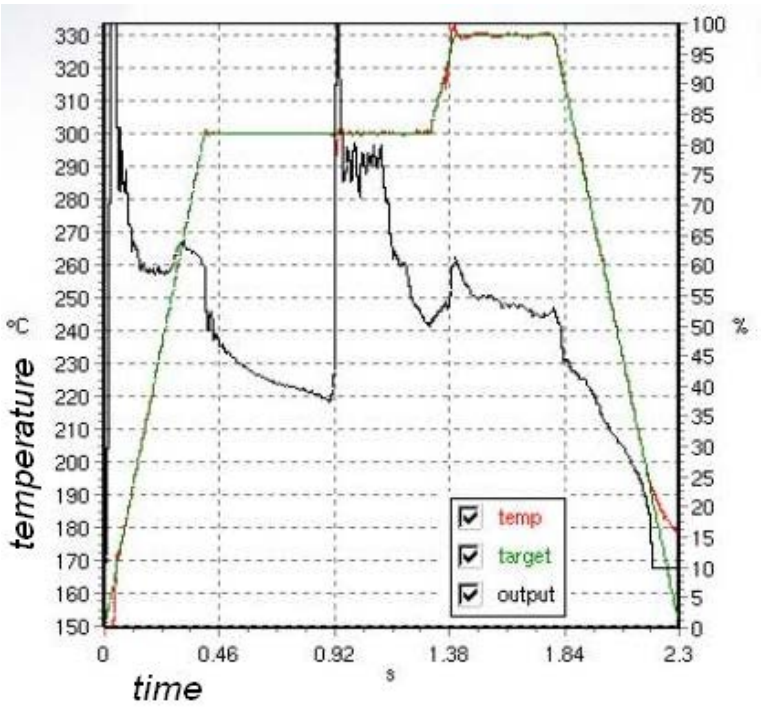


Fig. 3.1.25 Thermal profile for laser soldering

Initially, the pad is heated up to a temperature of 300°C. After approximately 1 second, it is switched on the solder wire feeder. The solder wire feeder is switched off after approx 1.4s. The process can be monitored on-line, allowing Pass/Fail decisions to be made. As an alternative to welding with tin solder wire, laser soldering with soldering paste is also possible. The paste must be applied with a dispenser. Squirting is largely prevented due to an optimized temperature program.

Advantages:

- ♦ Local heat absorption;
- ♦ Exact temperature control;
- ♦ On-line quality control;
- ♦ Larger quantities of heat can be emitted to small spots;
- ♦ Various points can be warmed up simultaneously or in succession using scanners.

Before soldering the surfaces have to be cleaned. A plasma technique is presented below: Ion bombardment cleans surfaces physically (sputtering) and, depending on the gas, also chemically. The contamination is vaporized and sucked away.

Applications of plasma cleaning (figure 3.1.26):

- ♦ Removing grease, oil, oxides or silicone
- ♦ Pre-treatment and preparation for bonding, soldering or gluing
- ♦ Pre-treatment for finishing metals

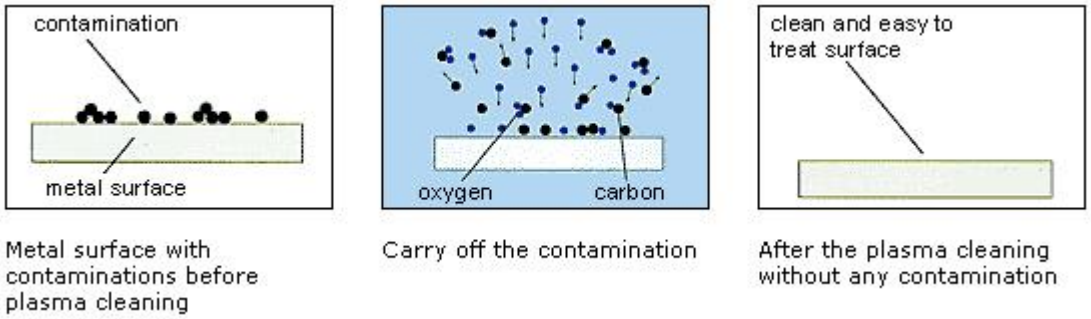


Fig. 3.1.26 Plasma cleaning steps

3.2 Package/Board assembling technologies

The documentation film from below, created by Johns Hopkins - Center for Educational Resources, presents the Self-Assembling Microdevices and Microfabrication.

- first, it presents the line between macroscale and nanoscale;
- second, the micro and nanoscale devices are introduced;
- to build them we need some phenomena:
  a) self-assembling;
  b) photolitography - build shapes at nanoscale.

Micro-devices and micro-fabrication
(http://www.youtube.com/watch?v=uyhxRIvw_cY&feature=PlayList&p=A78B809282540224&playnext=1&playnext_from=PL&index=10)

3.2.1 Chip-on-Board (COB)

Chip-on-Board (COB), refers to the semiconductor assembly technology wherein the microchip or die is directly mounted on and electrically interconnected to its final circuit board, instead of undergoing traditional assembly or packaging as an individual IC (figure 3.2.2). The elimination of conventional device packaging from COB assemblies simplifies the over-all process of designing and manufacturing the final product, as well as improves its performance as a result of the shorter interconnection paths. Figure 3.2.1 shows this approach with standard bonding techniques to form a Chip On Board (COB) used in an electronic game cartridge. The general term for COB technology is actually 'direct chip attachment', or DCA. Aside from circuit boards used for COB's, various substrates are available for use in DCA. There are, for instance, ceramic and glass ceramic substrates which exhibit excellent dielectric and thermal properties. Organic substrates that weigh and cost less while providing a low dielectric constant also exist. There are also flex substrates which, being pliable, have the ability to bend. DCA assemblies have received a number of other names aside from 'COB' based on these available substrates, e.g., chip-on-glass (COG), chip-on-flex (COF), etc.

The COB process consists of just three major steps:

- die attach or die mount;
- wire-bonding;
- encapsulation of the die and wires.

A variant of COB assembly, the flip-chip on board (FCOB), does not require wire-bonding since it employs a chip whose bond pads are bumped, which are the ones that connect directly to designated pads on the board. As such, FCOB's have their chips facing downward on the board (hence the name 'flip-chip'). Aside from encapsulation, it is also necessary to 'underfill' a flip chip to protect its active surface and bumps from thermo-mechanical and chemical damage.

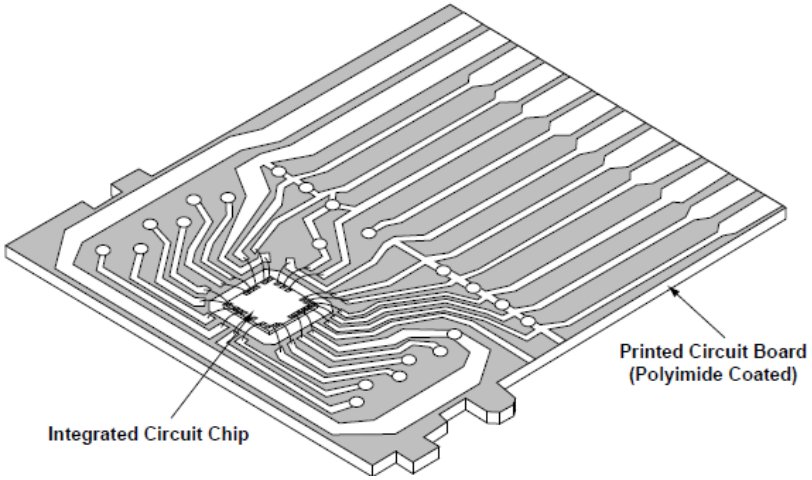


Fig. 3.2.1 Chip on board

Die attach basically consists of applying a die attach adhesive to the board or substrate and mounting the chip or die over this die attach material. Adhesive application may be in the form

of dispensing, stencil printing, or pin transfer. Die placement must be accurate enough to ensure proper orientation and good planarity of the die. This is followed by a curing process (such as exposure to heat or ultraviolet light) that allows the adhesive to attain its final mechanical, thermal, and electrical properties. After curing, organic contaminants must be removed either by plasma or solvent cleaning so as not to affect the wire-bonding process.

The wire-bonding process is similar to that used in traditional semiconductor assembly, i.e., thermosonic Au or Cu ball bonding or ultrasonic Al wedge bonding may be employed to connect wires between the die and the board or substrate. Chip-to-chip wire-bonding may also be done for COB assembly. Needless to say, the bond pads of the die and the board or substrate must be free of any contaminants and defects to ensure the formation of good and reliable bonds.

Finally, the die and bond wires are encapsulated to protect them from mechanical and chemical damage. Encapsulation is generally done by dispensing a liquid encapsulant material (usually epoxy-based) over the die and wires or by transfer molding. Encapsulants also need to undergo curing, the process of which depends on the type of encapsulant used.

Advantages offered by COB technology include:

- reduced space requirements;
- reduced cost;
- better performance due to decreased interconnection lengths and resistances;
- higher reliability due to better heat distribution and a lower number of solder joints;
- shorter time-to-market;
- better protection against reverse-engineering.

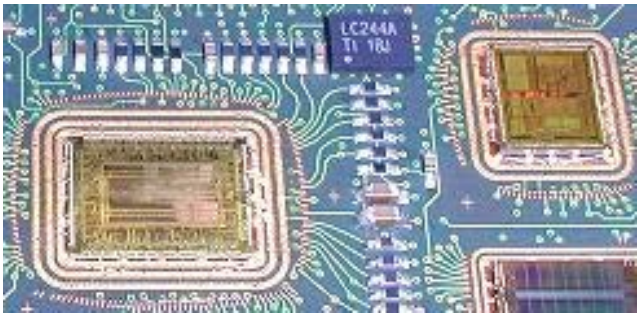


Fig. 3.2.2 COB assembly (chips directly wire-bonded to the PCB)

3.2.2 Chip Scale Packaging (CSP)

Originally, CSP was the acronym for Chip Size Packaging but very few packages are of true chip size. Therefore, the acronym is today usually used for Chip Scale Packaging. According to IPC’s standard J-STD-012, "Implementation of Flip Chip and Chip Scale Technology" a CSP shall have an area of no more than 1.2x (or 20%) the area of the original die size and is direct surface mountable. In contrast to most other package types, the name of the package type, "Chip Scale Packaging", contains no information about how the package is constructed, except for that it shall have approximately the same size as the chip. Therefore,

CSPs include component types with probably more dissimilar characteristics than any two other IC package types clearly manifesting the inaccuracy to look at CSPs as a homogenous group. Some packages look like miniaturised BGAs which names like miniBGA and µBGA indicate. Others have leads which give them properties similar to conventional leaded packages such as PLCCs. For this reason, CSPs are often classified based on their structure. These are:

- flex circuit interposer;
- rigid substrate interposer;
- custom lead frame;
- wafer-level assembly.

Examples of packages of these categories are given in figure 3.2.3.

The advantages and disadvantages of CSPs depend on what one compare with, standard surface mount or bare die assembly. Advantages toward standard surface mount technology:

- Reduced package footprint;
- Thin profile;
- Reduced weight;
- Better electrical performance;
- Area array distribution of connections (for most CSPs).

Advantages toward bare die assembly:

- Encapsulated package;
- Testable;
- Mountable with conventional assembly line;
- Die shrinkable without changing footprint;
- Some CSPs do not require underfill when mounted on organic substrates.

Disadvantages toward standard surface mount technology:

- Immature technology and poor infrastructure;
- Limited availability;
- Inspection of the solder joints is impossible without costly x-ray equipment;
- Limited reliability data available;
- Packages with high I/O counts require expensive high-density boards;
- Rework more difficult;
- Many CSPs require underfill when mounted on organic substrates;
- Potential high cost.

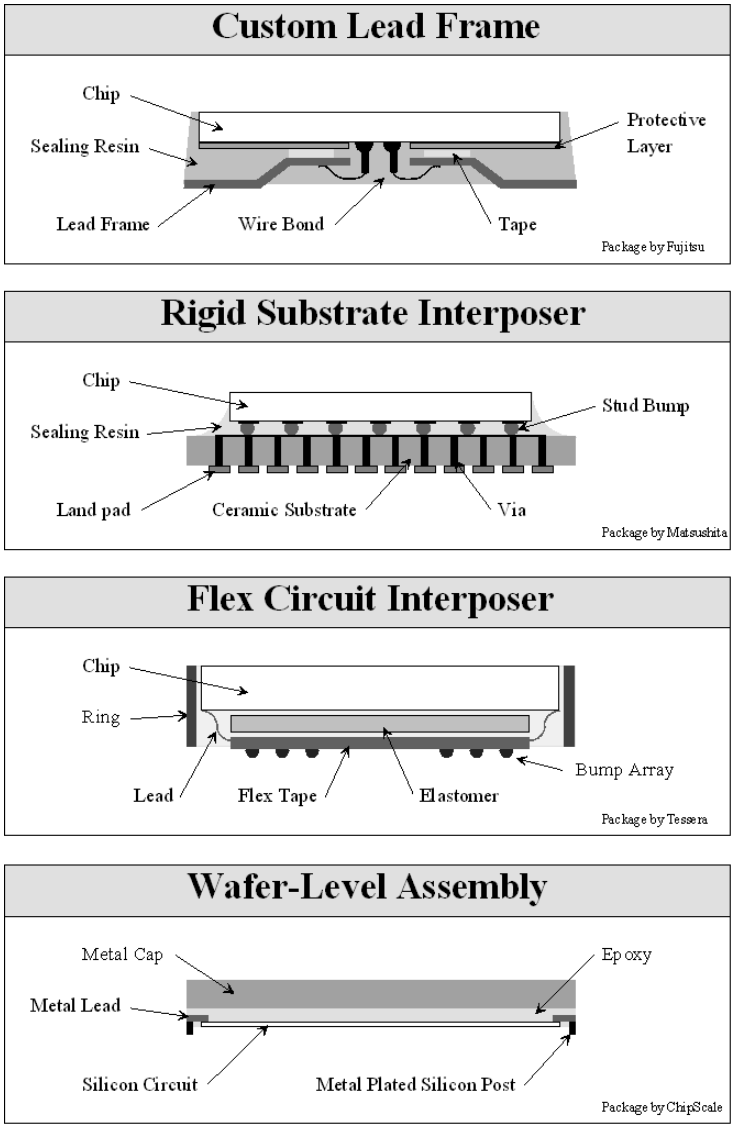


Fig. 3.2.3 Main CSP categories

Disadvantages toward bare die assembly:

- Somewhat inferior electrical and thermal properties.

The Institute for Interconnecting and Packaging Electronics Circuits (IPC) has released a standard dealing with CSP, J-STD-012 "Implementation of Flip Chip and Chip Scale Technology". This standard contains technology overview and information on design considerations, material properties and processes, mounting and interconnection structures, assembly processes, requirements for reliability, and standardisation. Although one of the advantages of CSPs compared to bare die assembling is the possibility to standardise, pitch and attachment site dimensions are still not standardised.

New CSP technology, Wafer Cap

Avago Technologies has developed a novel CSP technology that promises to enable SMT packages to reach the 100 GHz frequency range. Called Wafer Cap, it offers the same dimensions as an 0402 component and can reduce the amount of PCB space an RF device occupies by over 50%. Currently measuring 1.0mm x 0.5mm with a height of only 0.25mm, Wafer Cap packaged parts reduce the thickness of any assembly significantly. The use of vias removes the need for costly and performance limiting bond wires. Additionally, direct contact between the package substrate and the RF MMIC improves RF performance because it reduces the RF signal path and provides less resistance when compared to typical SMT designs. It also improves the heat transfer from the device to the assembly by removing the intervening package. The improved thermal condition and reduced number of bond wires greatly increase the reliability of the parts (figure 3.2.4).

Fig. 3.2.4 Wafer Cap SOT-343 case

By elimination of wire bonds in the packaging process gives the device the flexibility and simplicity to fit in a variety of positions in a wide range of RF architectures. With Wafer Cap, the air cavity created under the “lid” and immediately above the circuit makes it possible to achieve higher frequency ranges. No special tooling is required as assembly is done with standard SMT techniques. The devices can be directly soldered onto a board using standard soldering techniques. Traditional mass production “pick and place” or chip shooter machines can easily place a Wafer Cap packaged device onto any RF architecture. The differences between classic packaging technology and the revolutionary Avago’s technology are presented in figure 3.2.5.

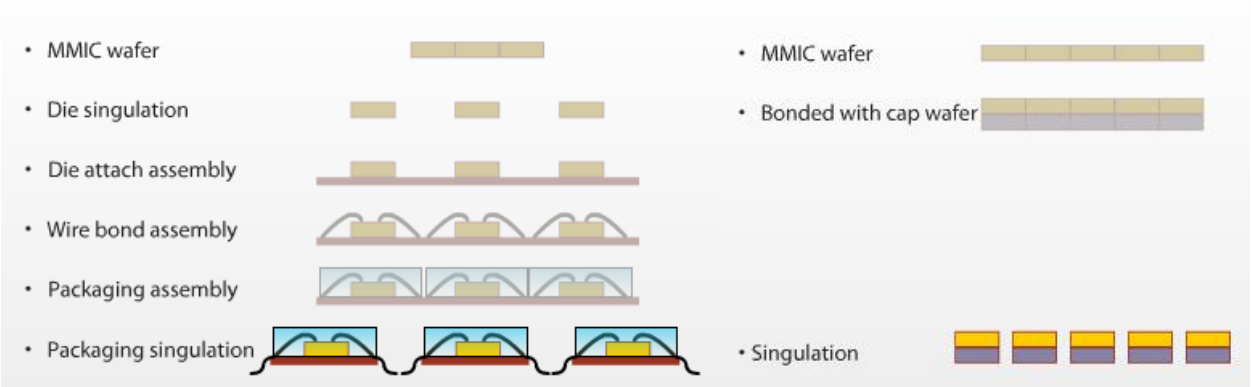


Fig. 3.2.5 Comparison between classic packaging technology and Avago’s technology

3.2.3 Wafer Level Packaging (WLP)

Wafer-Level Packaging (figure 3.2.6) refers to the technology of packaging an integrated circuit at wafer level, instead of the traditional process of assembling the package of each individual unit after wafer dicing. In conventional packaging there are two steps:

- ♦ wafer and singulation of that wafer into ICs;
- ♦ the subsequent packaging of these ICs into QFP, BGA, CSP or other packages.

In this new process, front-end IC fabrication and back-end IC assembly are performed at the wafer foundry. The basic concept is to take the wafer immediately after fabrication but before test, and form IC connections with a few more process steps with which to test and burn-in before singulating into packaged ICs.

Wafer-level packaging was born in the late 1990s and began to reach commercialisation in 2000. It has been adopted by the MEMS community because packaging of MEMS devices is a major cost issue. Most silicon-machined devices cannot be plastic packaged because molding compound would destroy movable parts or optical sensors. Optical packaging and most MEMS packages share the same basic problem (i.e., the device surface has to interact with the environment without any restrictions caused by the packaging, which at the same time must protect the device from the environment). Wafer-level packaging is possible if the active area of the sensor is on one side of the device and the contacts for the interconnect are placed on the backside of the image sensor chip.

There are at least four major WLP technology classifications in existence today, based on a study by Prismark and TechSearch International (source: www.future-fab.com):

1) Redistribution Layer and Bump technology;
2) Encapsulated Copper Post technology;
3) Encapsulated Wire Bond technology;
4) Encapsulated Beam Lead technology.

WLP is essentially a true chip-scale packaging (CSP) technology, since the resulting package is practically of the same size as the die:

1) Redistribution Layer and Bump technology, the most widely-used WLP technology, extends the conventional wafer fab process with an additional step that deposits a multi-layer thin-film metal rerouting and interconnection system to each device on the wafer. This is achieved using the same standard photolithography and thin film deposition techniques employed in the device fabrication itself.

This additional level of interconnection redistributes the peripheral bonding pads of each chip to an area array of underbump metal (UBM) pads that are evenly deployed over the chip's surface. The solder balls or bumps used in connecting the device to the application circuit board are subsequently placed over these UBM pads.

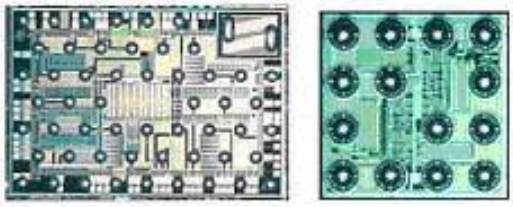


Fig. 3.2.6 Two WLP devices form Dallas-Maxim

Aside from providing the WLP's means of external connection, this redistribution technique also improves chip reliability by allowing the use of larger and more robust balls for interconnection and better thermal management of the device's I/O system.

Different companies using redistribution technology implement it using different materials and processes. Nonetheless, the sequence of steps required is more or less similar. The first layer put over the wafer to 'package' the device is usually a benzocyclobutane (BCB)-based polymer dielectric, to isolate the device circuitry from the rewiring system.

The rewiring metallization layer, usually Cu, Al, or a specially-developed alloy, is then deposited over this dielectric. This layer is then covered by another BCB dielectric layer serving as the solder mask. Underbump metallization is then put over the positions to be subsequently occupied by the solder balls. After the balls have been attached, flip-chip techniques are used to mount the WLP device onto the circuit board. Redistribution and bump technology is used by: Amkor (Ultra CSP™), Apack, Aptos, ASE (Ultra CSP™), ASAT Chipbond, Dallas Semi (2 lead), FCT (Ultra CSP™), Fraunhofer Institute, FuPo, Hitachi, Hyundai, National Semi (µSMD™), PacTech, Sandia Labs, Seiko Epson, SPIL (Ultra CSP™), Unitive (ExtremeCSP™).

2) Encapsulated Copper Post technology is very similar to redistribution and bump technology in the sense that the chip's bond pads are also rerouted into an area array of interconnection points. In this technology, however, these interconnection points are in the form of electroplated copper posts, instead of pads. These copper posts provide enough stand-off for the active wafer surface to be encapsulated in low-stress epoxy by transfer molding, exposing only the top portions of the posts where the solder balls will be attached. This WLP technology is supported mainly by Japanese companies (Casio, Fujitsu (SuperCSP™), IEP, Oki Electric, Shinko (SuperCSP™ license), Toshiba).

3) Encapsulated Wire Bond technology mainly pertains to the Wire-on-Wafer (WOW) technology developed by Form Factor. This technology employs a redistribution layer to reroute the device peripheral I/O's (bond pads) to meet the desired pitch. Using a modified gold ball bonder, gold ball-bumped micro-spring bond wires are formed on the redistributed pads. The technology for the micro-spring structures employed by this system originated from Form Factor's earlier efforts to come up with highly compliant contactors for fine-pitched probe cards. The micro-spring bond wires are then overcoated with electroless Ni/Au to make them more robust without sacrificing compliancy. This technology is used also by: Shinko, Hyundai, Infineon.

4) Encapsulated Beam technology includes a very diverse class of WLP techniques from wafer lamination to glass technology. Examples of this technology are Shellcase (ShellBGA™) and ShellOp™, and Tessera (WAVE™).

The flex tape WLP (figure 3.2.7) uses more conventional flexible tape and wire-bonding technologies to end up with a bumped WLP. A redistribution pattern is formed on copper-polyimide flex tape, and the patterned tape is then attached to the wafer with adhesive. The IC is then connected by wire-bonding its pads to the film as shown in figure. A liquid encapsulant is typically used to protect the wire-bonds and bond pads. The eutectic alloy solder balls are attached on 0.5 to 0.8mm pitch.

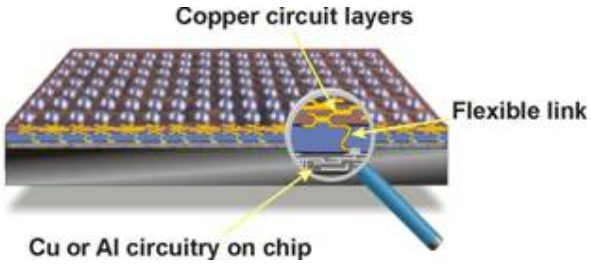


Fig. 3.2.7 Wafer level packaging structure

The benefits of WLP are:

- ♦ Smallest IC package size as it is a truly chip-size package (CSP);
- ♦ Lowest cost per I/O because the interconnections are all done at the wafer level in one set of parallel steps;
- ♦ Lowest cost of electrical testing as this is done at the wafer level;
- ♦ Lowest burn-in cost as burn-in is done at the wafer level;
- ♦ Potentially eliminates underfilling with organic materials around the solder joint;
- ♦ Enhances electrical performance because of the short interconnections.

3.2.4. Integrated circuit (IC)

Packaging the IC chip is a necessary step in the manufacturing process because the IC chips are small, fragile, susceptible to environmental damage, and too difficult to handle by the IC users. In addition, the package acts as a mechanism to “spread apart” the connections from the tight pitch (centre to centre spacing of two parallel conductors) on the IC die to the relatively wide pitch required by the Printed Circuit Board (PCB) manufacturer.

The pad pitch on the IC chip is typically 0.006 inch (6 mils or 152μm). This spacing is already much larger than the 2 to 8 microns (0.08 to 0.31 mils) pitch of the wiring (metallization) on the IC chip. But PCB wiring requires an even larger pitch, usually between 40 and 100 mils. The package acts as a “bridge” between the two sizes, effectively spreading apart the spacing from the IC chip dimensions to the PCB dimensions, as shown in figure 3.2.8. Early packages were required to expand the pitch to the very large board pitch required for economical manufacture of PCBs used in commercial applications. In addition, the packages were mounted on the PCBs through plated holes, typically on 100 mil pitch. Three package types were used,

ceramic and metal for hermetically sealed requirements and plastic for general commercial use. Hermetically sealed parts are ones where the IC chip is enclosed in a sealed compartment and outside chemicals and gases cannot reach the die. According to the assembling technology, there are through hole device (THD) and surface mount device (SMD) packages.

Common through hole device packages are:

- ♦ Single In-Line (SIL) (figure 3.2.10/a);
- ♦ Dual In-Line (DIL);
- ♦ Pin Grid Arrays (PGA);
- ♦ Ceramic flatpack (figure 3.2.10/d).

Common surface mount device packages are:

- ♦ Small Outline IC (SOIC);
- ♦ Quarter Size Small Outline Package (QSOP);
- ♦ Leadless Chip Carrier (LCC);
- ♦ Plastic Leaded Chip Carrier (PLCC);
- ♦ Ball Grid Array (BGA);
- ♦ Plastic Quad Flat Pack (PQFP)
- ♦ Quad Flat No leads (QFN).

Most used package for through hole ICs are Plastic Dual In-Line Package and its ceramic version, DIP. The lead configuration consists of two rows of leads, both with 100 mil pitch. The plastic DIP is shown in figure 3.2.9. The side-braze and cerdip packages are its hermetic alternatives. The cerdip is considerably less expensive than the side-braze. Both packages are available with quartz windows in the top for EPROM devices so the chip can be erased with ultraviolet light.

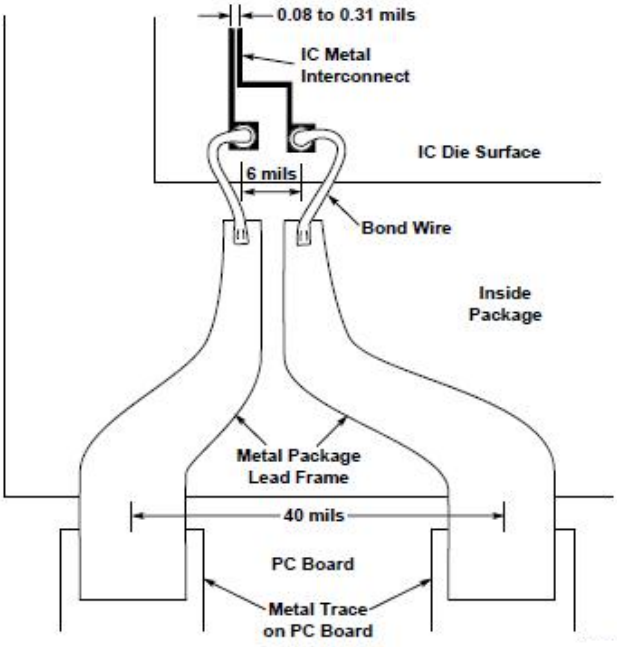


Fig. 3.2.8 IC Chip to PCB Lead Spacing

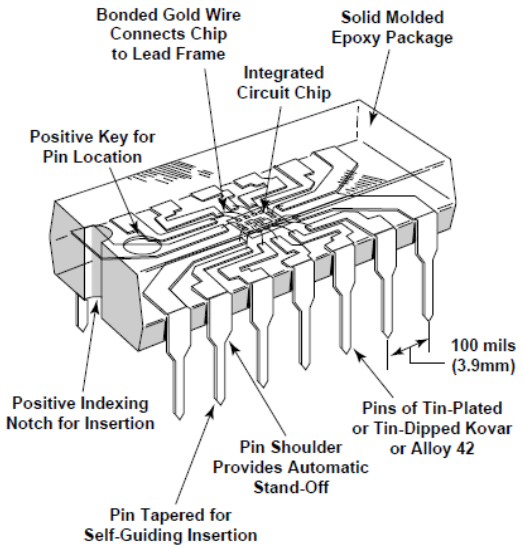


Fig. 3.2.9 Plastic Dual In-Line Package

To further reduce the PCB cost, which goes up as the wiring pitch is reduced, some manufacturers use the packages with staggered leads, such as the QUIP (figure 3.2.10/b); or Multiwatt (figure 3.2.10/c).

While THDs have somehow the same form of the lead, SMDs have different kind of leads: lap, butt and J-form (figure 3.2.11).

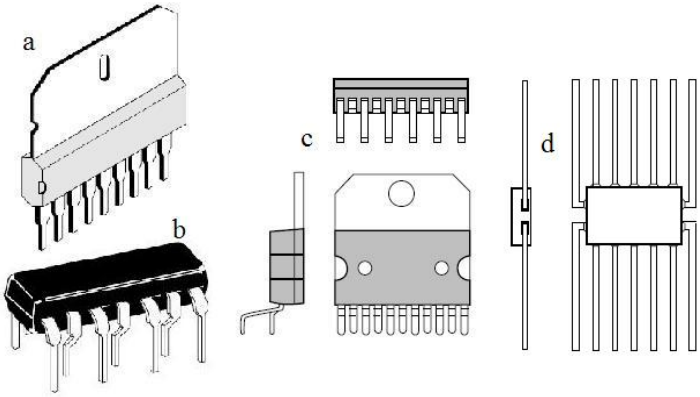


Fig. 3.2.10 Different through hole IC packages: a) SIP, b) QUIP, c) Multiwatt 11, d) ceramic flatpack

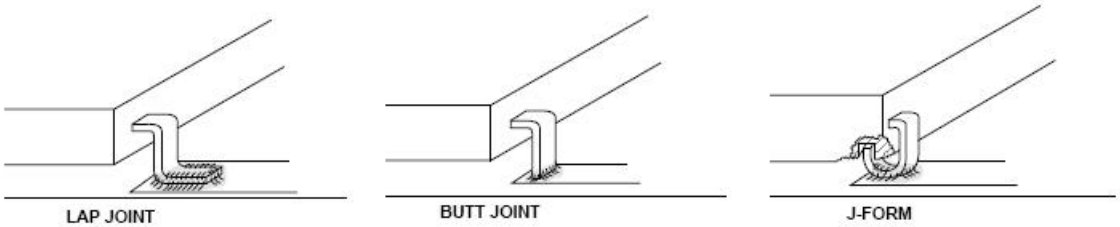
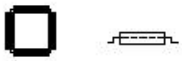


Fig. 3.2.11 Types of leads

A comparison between package types is presented in Table 3.2.1.

Package Type	Description	Advantages	Disadvantages
Dual-in-Line 	0.100in. Pin Centers 0.125in. Pin Length 0.160in. Body Thickness 0.300in. to 0.900in. Body Width	Capabilities Generally Exist Lowest Implementation Cost Minimum Engineering Effort Well-Established Reliability Database	Pin Count Limited to Less Than 64 I/O Lines Not Surface Mountable
SOIC (Small-Outline IC) 	0.050in. Pin Centers 0.030in. Pin Length (Solderable) 0.098in. Body Thickness 0.155in and 0.300in. Body Width	Surface Mountable Lowest Material Cost Allows Magagine Handling Soldering/Rework (Versus Quad Flat Pack)	Significant Equipment Design and Tooling Handling and Test More Difficult Board Routing/Soldering/ Rework of 0.050in. Pin Centers Reliability Questions
Quad Flat Pack 	0.050in. Pin Centers 0.030in. Pin Length 0.095in. Body Thickness Variable Body Width	Low Materials Cost Solder Joints Visible (Versus Chip Carrier)	Process and Test Modifications Needed Pin-Count Limitations Handling Difficult Board Routing More Complex Soldering/Rework of 0.050in. Centers Reliability Concerns
Chip Carrier 	0.050in. Pin Centers 0.030in. and 0.060in. Standoff 0.100in. Body Thickness JEDEC-Compatible Sizes	High Pin Counts Possible Surface Mountable Less Stressed Than Quad Flat Pack	Development Time and Cost Board Routing/Rework More Difficult Solder-Connect Technology and Joint Reliability
Plastic Chip Carrier 	0.050in. Pin Centers 0.100in. Pin Lengths 0.145in. Body Thickness JEDEC-Compatible Sizes	Surface Mountable Minimum Engineering Effort Low Materials Cost	Technology Compatible With Pin Counts Under 84 Leads Board Routing/Rework of 0.050in. Centers

Tab. 3.2.1 Comparison between package types

3.2.5 Stacked-Die packages

Three-dimensional (3D) packaging is expected to emerge as a dominant performing solution in the electronic/chip packaging industry. Its performance promises to drive efforts across the entire supply chain to successfully deploy it.

New analysis in this field finds that 3D packaging technology will be the key in catering to the ever-increasing miniaturization demands from application sectors that include consumer electronics, game consoles, and a wide range of high-speed memory devices. Looking beyond successful solutions such as system on chip (SoC), the electronic/chip packaging industry has steadily started exploring various forms of system in package (SiP)-based solutions.

Currently, the industry focuses on interconnect technologies, signal integrity issues, and manufacturing capabilities. Resolving all challenges with regards to 3D system design remains very important to drive this technology efficiently across the supply chain.

As micro-electro-mechanical-systems (MEMS) ICs satisfy more functions and proliferate, packaging them into high-density form factors like 3D becomes more of a challenge than conventional ICs. To suppress costs and make them more competitive in the market, they need high-density packaging. MEMS devices are essentially “machines” that involve motion, not transistors.

Most MEMS devices are integrated in a package by attaching the MEMS die to a CMOS IC via wire-bonding or by placing the MEMS die above a CMOS silicon wafer. Nevertheless, manufacturing processes that involve 3D MEMS packaging have proven to work by taking advantage of wafer-level packaging (WLP). One such example comes from Innovative Micro Technology (IMT), which successfully made micro-fluidic and other MEMS functions using through-silicon vias (TSVs).

There are different motivations for the development of 3D IC solutions:

- Form factor: to increase density (achieving the highest capacity / volume ratio): TSV interconnect is the ultimate solution to overcome the space limitations of POP and Wire Bond packages;
- Increased electrical performances: to shorten interconnect length (device speed), to improve electrical performances (reducing electrical parasitances due to RC delays in RF and DRAM applications) and to strongly reduce chips power consumption;
- Heterogeneous integration: to integrate different functional layers (RF, memory, logic, MEMS, imagers, exotic substrate material) based on different optimized process nodes.
- Cost: at some point, 3D integration will be cheaper than shrinking furthermore 2D design rules.

Trend is to move from 3D stacking & 3D flexible configurations to 3D Ics (figure 3.2.12):

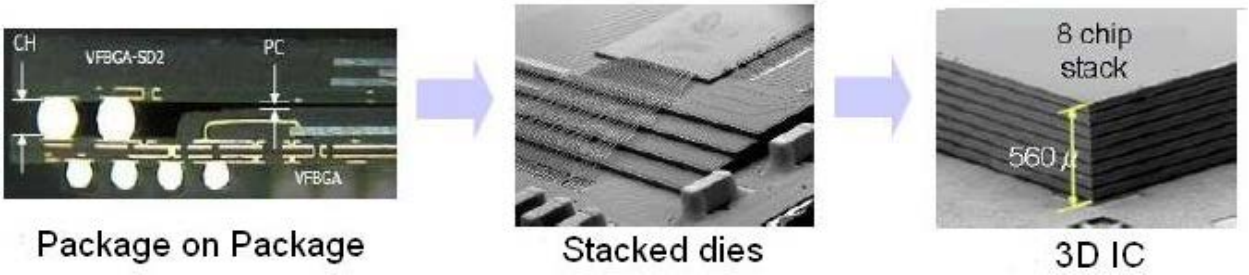


Fig. 3.2.12 Trend in 3D packaging

The broad range of 3D packaging is presented in figure 3.2.13.

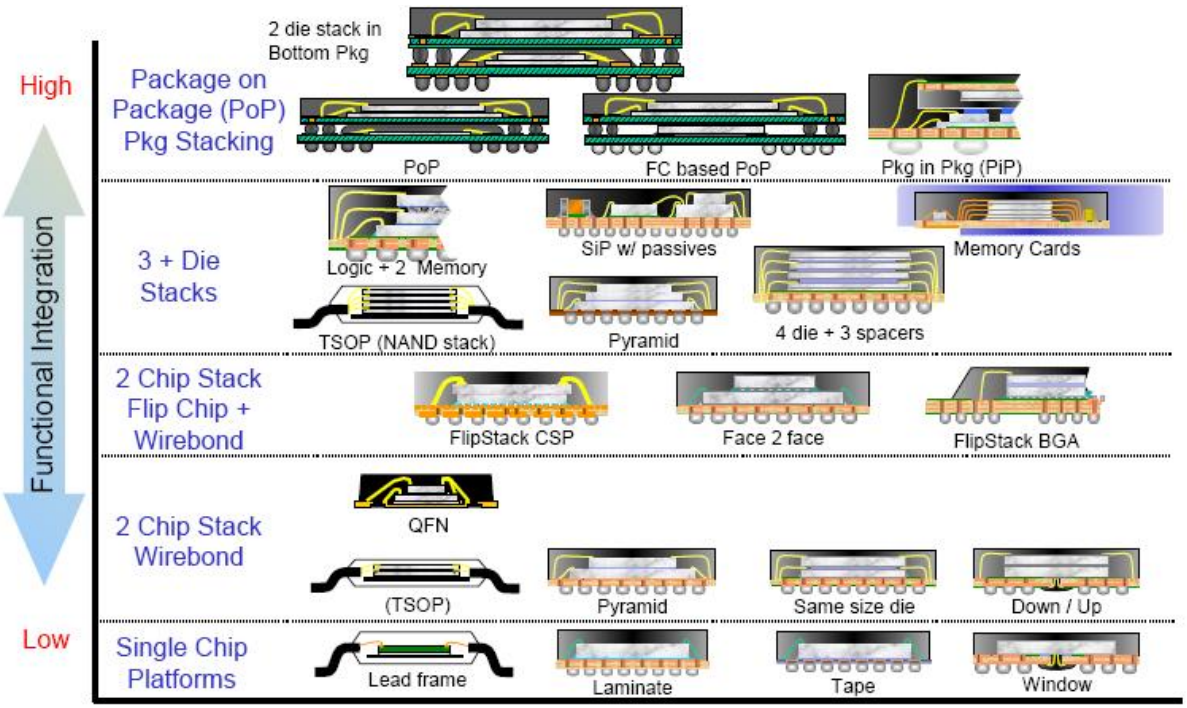


Fig. 3.2.13 Broad range of 3D packaging

Stacking die uses established infrastructure and materials. It provides the smallest footprint, the lowest profile and lowest cost package. Stacking die is most popular in BGA while in leadframe packages (QFP, QFN) is growing.

3D packages come with some problems that must be solved:

- thermal problem: the increase of chips grows the temperature, the smaller size package increases the thermal resistance, the high speed transmission and high density mounting impose restriction on T_j and T_a; these requirements need a better interposer development (e.g. metal-core), new technology in thermal problem, development with consideration of environment use;
- reliability;
- warpage behaviour during IR reflow.

Stacked Multi-Chip Package (Stacked MCP) is one of the most suitable chip scale packages for wireless applications. Its advantage is the compact stacked chip configuration. In the Flash memory and SRAM configuration, the pin layout can accomodate a 128 MB combination. Typical package construction consists of two die back lapped down to 100µm and total package height is only 1.2mm. Different combinations of Flash and SRAM can be mounted in this package up to package size 10.4 x 10.8mm.

Stacked MCP supports packaging solutions up to 8 die stacked using flip-chip interconnection and stacked wire bonded die.

Basic package structure and materials (figure 3.2.14):

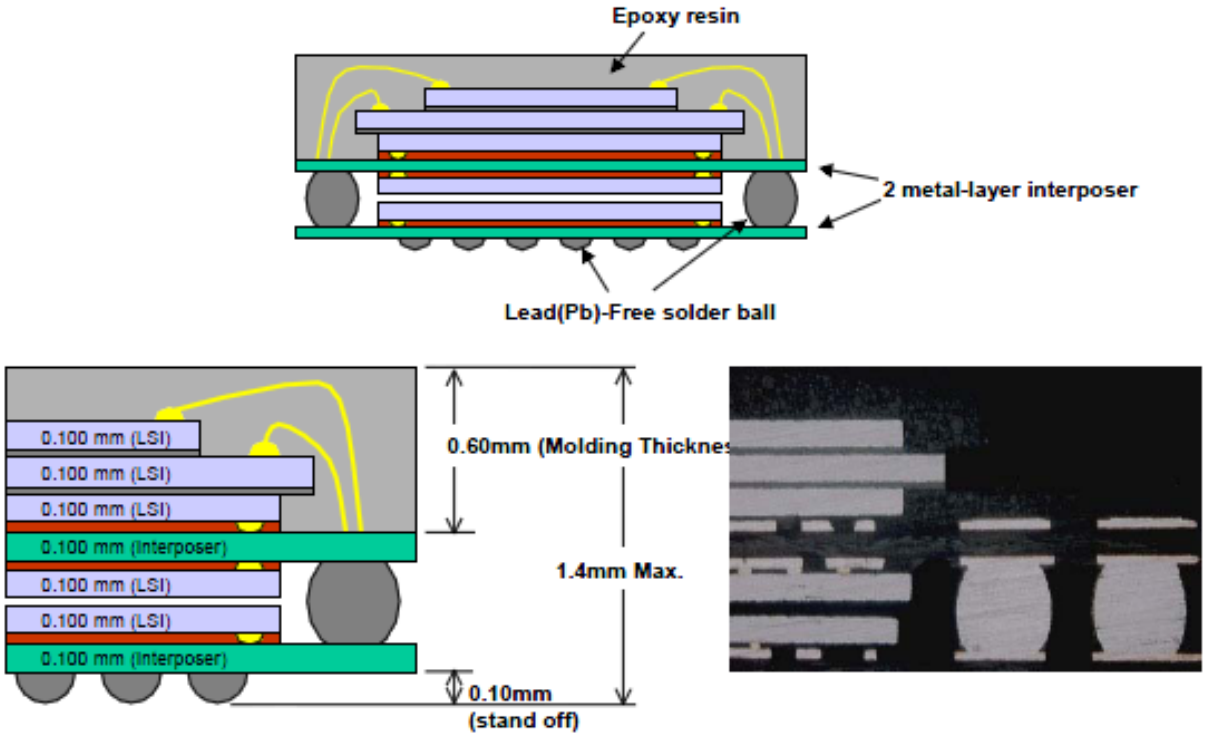


Fig. 3.2.14 Basic package structure of a stacked MCP

3.2.6 Quad Flat Package (QFP)

A QFP is an integrated circuit package with leads extending from each of the four sides. It is used for surface mounting (SMD); socketing is rare. There are versions having from 32 to 304 pins with a pitch ranging from 0.4 to 1.0mm. Special cases include LQFP (Low profile QFP) and TQFP (Thin QFP).

The basic form is a flat rectangular (often square) body with leads at four sides but with numerous variations in the design. These differ usually only in lead number, pitch, dimensions, and materials used (usually to improve thermal characteristics). A clear variation is Bumpered Quad Flat Package (figure 3.2.15) with extensions at the four corners to protect the leads against mechanical damage before the unit is soldered.

Fig. 3.2.15 A Cyrix Cx486SLC in Bumpered Quad Flat Package format

- ♦ BQFP: Bumpered Quad Flat Package
- ♦ BQFPH: Bumpered Quad Flat Package with heat spreader
- ♦ CQFP: Ceramic Quad Flat Package
- ♦ FQFP: Fine Pitch Quad Flat Package
- ♦ HQFP: Heat sinked Quad Flat Package
- ♦ LQFP: Low Profile Quad Flat Package
- ♦ MQFP: Metric Quad Flat Package
- ♦ PQFP: Plastic Quad Flat Package
- ♦ SQFP: Small Quad Flat Package
- ♦ TQFP: Thin Quad Flat Package
- ♦ VQFP: Very small Quad Flat Package
- ♦ VTQFP: Very Thin Quad Flat Package

Some QFP packages have an Exposed Pad. The exposed pad is an extra pad underneath or on top of the QFP that may act as a ground connection and/or as a heat sink for the package. The pad is typically 10 or more mm², and with the pad soldered down onto the ground plane heat is passed into the PCB. This exposed pad also gives a solid ground connection. These type of QFP packages often have a -EP suffix (e.g. a LQFP-EP 64), or they have an odd number of leads, (e.g. a TQFP-101).

A standard QFP package is shown in figure 3.2.16.

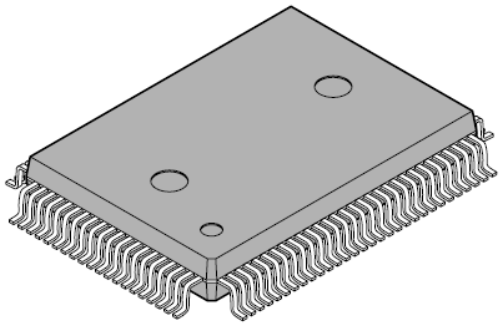


Fig. 3.2.16 100-pin standard QFP with gull leads

3.2.7 Quad Flat No leads (QFN)

Quad Flat No leads or MLF packages (figure 3.2.17) physically and electrically connect integrated circuits to printed circuit boards. QFN is a surface mount plastic package that is similar to the Quad Flat Package, but the leads do not extend out from the package sides. This is a near CSP plastic encapsulated package made with a planar copper lead frame substrate. Perimeter lands on the package bottom provide electrical connections to the PCB. The package includes an exposed thermal pad to improve heat transfer out of the IC (into the PCB). Heat transfer can be further facilitated by metal vias in the thermal pad. This simple and typically low cost packaging is still the best solution for many applications and is ideal for analog power switching, automotive and infrastructure applications. A section view of a QFN package is presented in figure 3.2.18. The connection between the chip and the lead frame is made by bonding a gold wire of 1 - 2 mil in diameter.

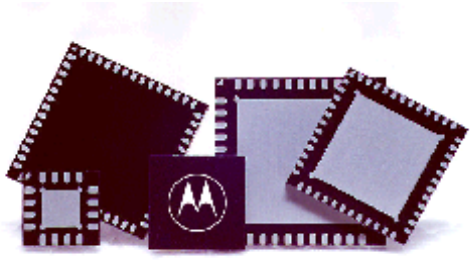


Fig. 3.2.17 QFN package

Advantages of QFN package:

- reduced lead inductance;
- small sized "near chip scale" footprint;
- thin profile;
- low weight;
- exposed copper die-pad technology offers good thermal and electrical performance.

It also uses perimeter I/O pads to ease PCB trace routing.

There are currently two types of QFN packages:

♦ **Air-Cavity QFN**s, with an air cavity designed into the package;
♦ **Plastic-Moulded QFN**s with air in the package minimized.

Less-expensive plastic-moulded QFNs usually limited to applications up to ~2-3GHz. It is usually composed of just 2 parts, a plastic compound and copper lead frame, and does not come with a lid. In contrast, the Air-Cavity QFN is usually made up of 3 parts; a copper leadframe, plastic-moulded body (open, and not sealed), and either a ceramic or plastic lid. It is usually

more expensive due to its construction, and can be used for microwave applications up to 20-25GHz.

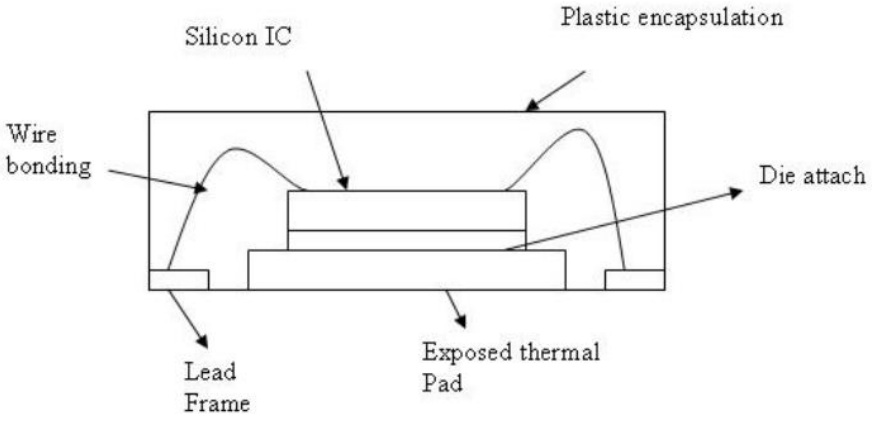


Fig. 3.2.18 Cross section of a QFN package

Here are the features of a QFN package from Freescale:

- Cost-reduced, smaller packages with high thermal dissipation/low Ron;
- Package size of 2x2mm up to 12x12mm;
- Thin profile of 0.65mm to 1.00mm;
- Designed with a single exposed die pad (flag) depending on device requirements and intended application.

QFN package family

Power Quad Flat No-Lead (PQFN). The PQFN package is a surface mount plastic package with lead pads located on the bottom surface of the package. The PQFN is ideal for analog power switching, automotive and infrastructure applications. Features:

- ♦ Cost-reduced, smaller packages with high thermal dissipation/low Ron;
- ♦ Designed with a single exposed die pad (flag) or multiple exposed die pads depending on device requirements and intended application;
- ♦ The industry standardization committee, JEDEC, has given a registered designator of MO-251 to describe the family of single exposed pad PQFN packages.

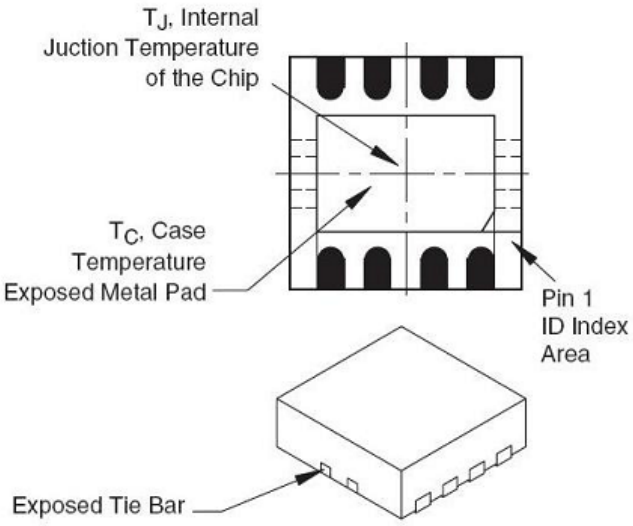


Fig. 3.2.19 DFN package (Microchip)

Dual Flat No Lead. In the same family of packages could be counted the Dual Flat No Lead (DFN), or Micro Dual Flat No Lead (uDFN) which is a style of integrated circuit package that has no pins or wires but uses contact pads instead (figure 3.2.19). EIAJ and JEDEC have their respective design guidelines and structure description for this package. Freescale adopted the uDFN-EP / QFN-EP package design rules under JEDEC, document MO-229 and MO-220 respectively

Singulation Method

There are two main singulation methods for uDFN / QFN packages, punch and saw. Punch singulation is used on individually molded packages, while saw singulation is performed on Molded Array Packages, similar to wafer singulation. The cross-sectional profiles for each are different and are illustrated in figure 3.2.20. For uDFN/QFN packages, Freescale offers two different lead terminal types: “E” and “S” styles. The “E” version follows JEDEC MO-220 (QFN) and MO-229 (uDFN) design guidelines. The lead extends to the package perimeter, where the lead ends are fully exposed to the side of the package (see figure 3.2.20/a). A solder fillet is expected to form and should be visible on the PCB after the solder reflow process. However, a solder fillet is not guaranteed and is dependent upon the stencil design and paste volume.

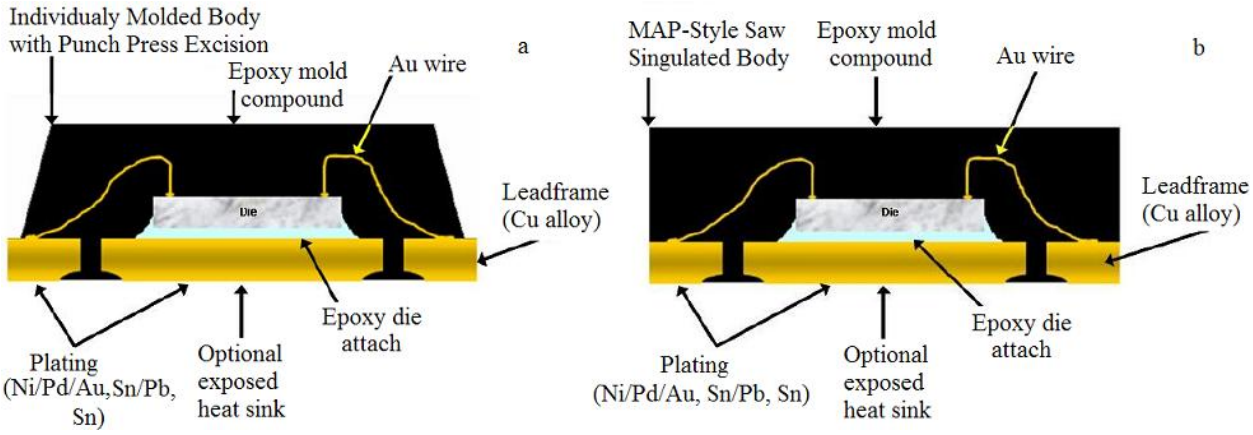


Fig. 3.2.20 Cross section view of: a) Punch QFN, b) Saw QFN

The “S” style is a Freescale version based on JEDEC MO-220 / MO-229, with an exception in the lead end feature. The lead end is slightly recessed from the package perimeter due to a ½ etched lead frame (see figure 3.2.20/b). No solder fillet is expected after the solder reflow process. The “S” style lead frame design is the Freescale standard. The “E” style can be considered, but the “S” style is better suited to meet the burr requirements during singulation.

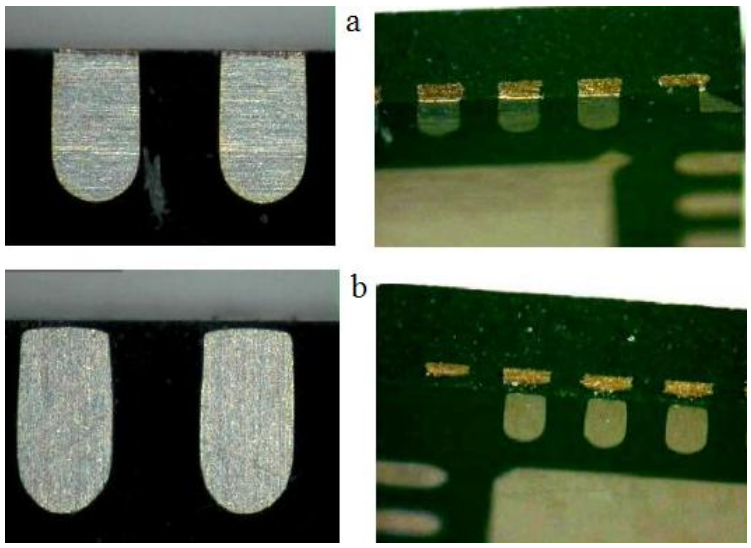


Fig. 3.2.21 MAP uDFN/QFN: Left-Bottom View, Right-Tilted to Show Side and Bottom Views: a) "E" Version, b) "S" Version

Process flow

The MAP style uDFN / QFN package process flow is illustrated in figure 3.2.22. The illustration displays the difference between the Quad Flat Pack (QFP) and QFN process flows. The QFN package process flow is dependent upon the material set and factory. The Freescale MAP style uDFN/QFN is assembled using pre-plated NiPdAu lead frames and does not require any post plating process. For the punch singulated QFN process, the tape and de-taping operations displayed in Freescale MAP Style uDFN/QFN Process Flow are not required.

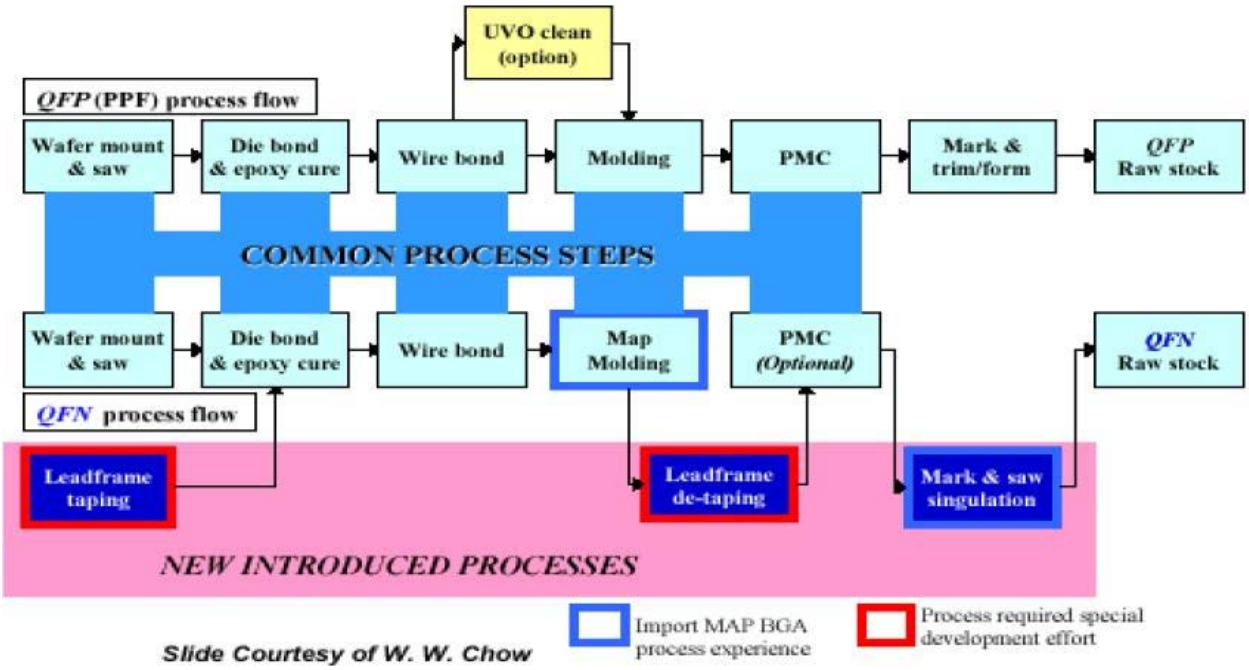


Fig. 3.2.22 Process flow for QFN (Freescale)

3.2.8 Ball Grid Array (BGA)

Basics

The demanding space and weight requirements of personal computing and portable electronic equipment have led to many innovations in IC packaging. Leaded surface mount devices are constantly pushing the manufacturing capabilities of leading board manufacturers to finer and finer lead pitch geometry's to increase I/O density and reduce board space. This requirement has lead to new package concepts to be suited to low cost, high volume applications, where package size and performance is of major importance. One of these concepts was the Ball Grid Array (BGA). The BGA package is composed of three basic parts (figure 3.2.23):

- the bare chip;
- the BGA substrate;
- the interconnection matrix.

Depending on the package style, the bare chip may be affixed to the BGA substrate either face-up or face-down. The interconnection matrix then connects the bare chip to the BGA substrate using wire-bond, tape-automated-bonding (TAB), or direct attach flip-chip style connections (figure 3.2.24).

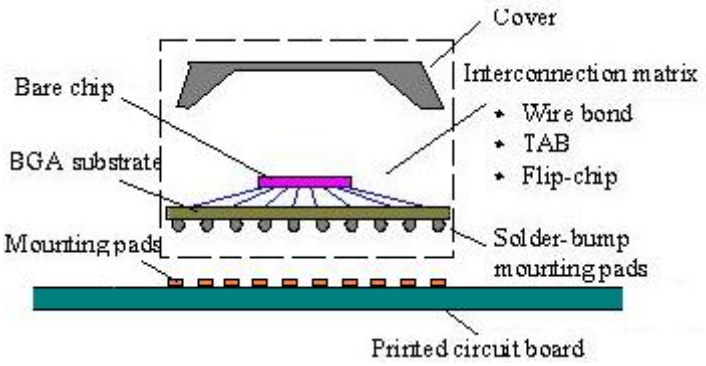


Fig. 3.2.23 BGA package concept

The BGA substrate, which is really a miniature multi-layer PCB with traces and microscopic through-hole vias, conveys the signals to the underlying printed circuit board through an array of solder-bump attachment pads on its bottom surface. The BGA is descended from the Pin Grid Array (PGA), which is a package with one face covered (or partly covered) with pins in a grid pattern. In a BGA, the pins are replaced by balls of solder stuck to the bottom of the package. Balls or pins are used to conduct electrical signals from the integrated circuit to the printed circuit board (PCB) on which it is placed.

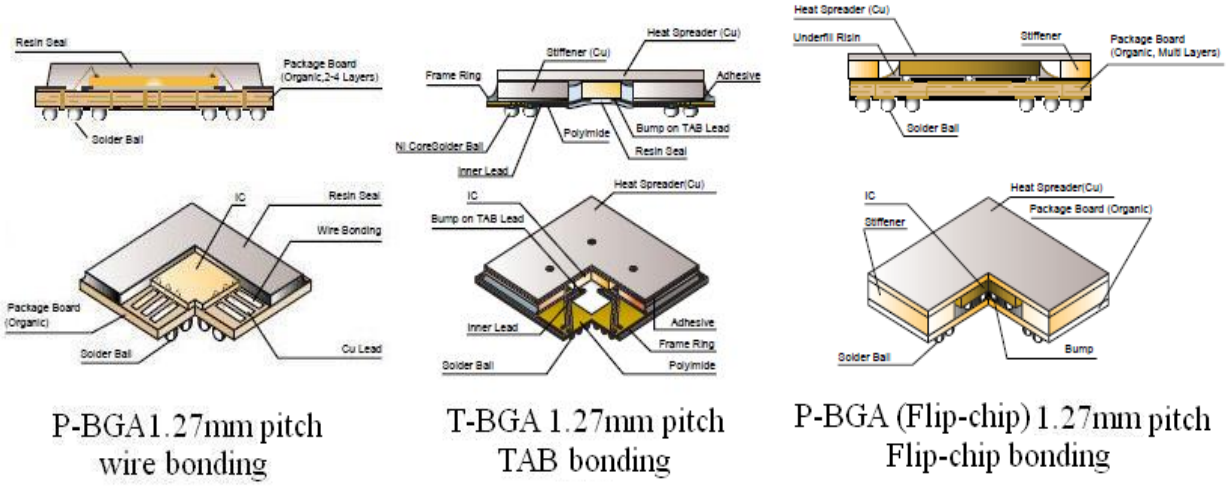


Fig. 3.2.24 Types of BGA

At 0.4 to 0.5mm pin pitch, the race to finer surface mount lead pitches has hit several technical and economic walls. Manufacturing anything smaller will significantly impact PCB yield and push board costs above acceptable levels for the highly competitive and cost conscious electronics industry. Avoiding problems such as bent leads and solder bridging become significant manufacturing challenges. Additionally, electrical problems such as crosstalk become a major issue due to the length and close pitch of the leads on surface mount packages. Alternatively, BGA packaging uses relatively wide “pad to pad” pitch rules and when coupled with existing PCB manufacturing processes result in high yields. The “array” approach improves I/O density and reduces the board space consumed by the device. Figure 3.2.25 shows two 0.15mm (6 mil) line routing techniques.

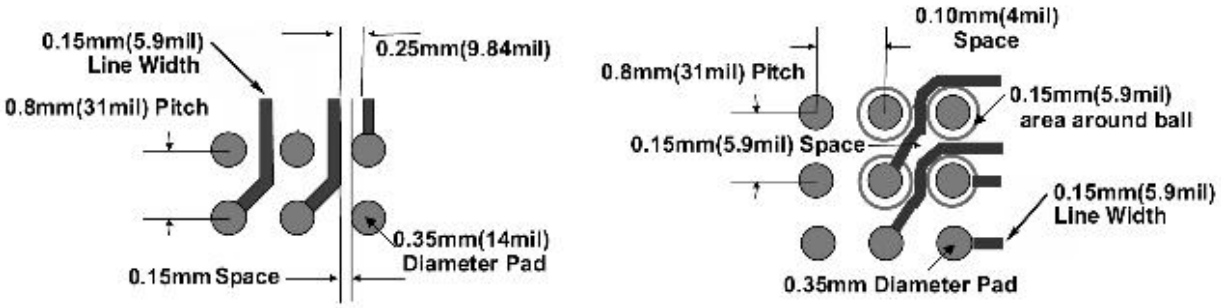


Fig. 3.2.25 Line routing techniques on BGA

The advantages of BGA:

- miniaturisation;
- higher interconnect density;
- low inductance leads;
- lower assembly cost;
- self-alignment during reflow;
- lower thermal resistance.

The disadvantages of BGA:

- expensive X-Ray inspection of solder joints;
- higher costs (molding, ceramics, polyimide, BT);
- moisture sensitivity (“pop-corn” effect);
- excessive PWB warpage during reflow;
- difficulty in rework and cleaning (flux residue);
- non-compliant leads.

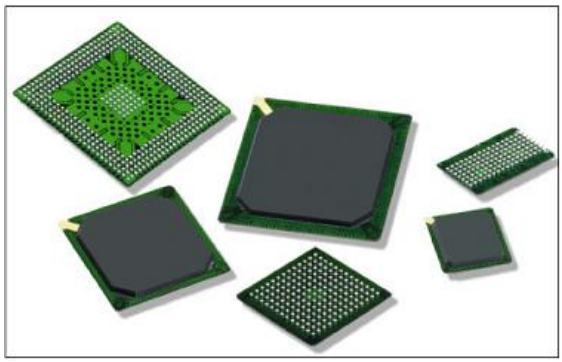


Fig. 3.2.26 Different types of BGA packages

Motorola invented BGA interconnect technology in the early 1990s. Now numerous variants are in high volume production that address specific market requirements. Their applications run from hand held electronics to computing to automotive environments. Currently, there are producing seven major families of BGA packages (Table 3.2.2). Different types of BGA packages are shown in figure 3.2.26.

Type	Description	Shape
CBGA	Ceramic Ball Grid Array	Square, rectangle
CCGA	Ceramic Column Grid Array	Square, rectangle
PBGA	Plastic Ball Grid Array	Square, rectangle
TBGA	Tape Ball Grid Array	Square
LBGA	Low-Profile Ball-Grid-Array	Square, rectangle
TBGA	Thin-Profile Ball-Grid-Array	Square, rectangle
VBGA	Very-Thin-Profile Ball-Grid-Array	Square, rectangle

Tab. 3.2.2 Major families of BGA packages

µBGA

The Micro Ball Grid Array package (µBGA) is considered a "chip size" package (CSP). A chip size package is generally defined as a package which does not exceed the die size by greater than 20%. µBGA has many advantages over other CSP alternatives, for example, easy board assembly, temperature cycle tolerance, no underfill, solder joint reliability and moisture resistance. An additional advantage of µBGA is that it can be used with today's PCB surface mount device assembly processes. Lacking leads, the µBGA package has reduced coplanarity and handling issues. During reflow, the solder balls are self centring (within limits), thus reducing placement problems during surface mount. The µBGA package is used for space constrained applications. The µBGA package offers the smallest flash package foot print available and has excellent solder joint reliability characteristics.

Micro BGA's and CSP's are actually the same thing! Tessera Inc. trademarked the term µBGA, and CSP is the term used by the rest of the industry.

Materials

Substrate. There are two basic materials for BGA substrate: organic (FR-4) and ceramics. The organic substrate typically comprises a reinforced polymer laminate material, such as bismaleimide triazine (BT), or a polyimide resin. Organic (plastic) substrate could reduce cost, primarily due to the simpler manufacturing steps.

The ceramic substrate is the Hi-CTE Glass Ceramic. Alumina ceramic substrate offers better moisture resistance, electrical insulating property and lower coefficient of thermal expansion (CTE) than organic substrate. CTE is low enough so that there is only a small thermo-mechanical mismatch between chip and substrate. This means that underfill is not required for thermo-mechanical enhancement, at least for smaller die. Another important feature of ceramic is high-temperature stability as well as superior thermal conductivity. Ceramic can handle 300^{o}C or higher, a valuable feature for a chip carrier. Some materials conduct heat better than aluminium

and are therefore ideal for heat dissipation. The high-temperature performance of ceramic allows higher-melting solders to be used for chip attach so melting will not occur when the package is soldered to the printed wiring board (PWB).

Although ceramic has become less popular because of higher cost, it has been used to build FCBGAs. AMD, for example, has used ceramic BGAs for the K6 and K7 microprocessors. The difference in the PCB layout design will reflect in bigger pads size and in larger solder paste pads in this substrate than in the FR-4 substrate.

Encapsulant. Encapsulation materials are used to absorb the coefficients of thermal expansion mismatch found between the solder balls, the die and the printed wiring board. This property allows the parts to show the highest level of reliability. An underfill encapsulant, typically an epoxy composition, wicks under a chip by capillary action, and then is cured. It provides mechanical reinforcement to the solder joints, increasing life of the chip. For BGA underfill encapsulation, the proper encapsulant must be easy to handle and process, providing the required reliability. Parameters such as storage conditions, pot life, dispensability, underfill flow speed and cure time are paramount to handling and processing.

Pot life is the useful life of an underfill encapsulant after it is removed from the freezer and thawed, typically determined by the ability to dispense uniform quantities at uniform speeds. Thus, viscosity must be stable over the length of the pot life. One definition of end of pot life is the time for viscosity to rise 10 percent.

If board value is high, a reworkable underfill might be used. In such cases, ease of rework is important. A BGA underfill encapsulant has lower viscosity and density than a typical flip chip encapsulant. This allows a BGA encapsulant to flow much faster, desirable since the volumes to be filled are much larger for a BGA.

Void-free encapsulation, drop test life and thermal cycle life are important issues in reliability of handheld devices.

As encapsulant there are used:

- Silicones: Silicone encapsulants are based on a stable siloxane backbone with excellent stress relief and other properties under extreme temperatures (-40 to 200°C). Addition cure ensures no byproducts.
- Epoxies: Hard, usually opaque, materials that offer adequate moisture resistance. They exhibit good high-temperature stability, but they tend to degrade at low temperatures. They are stiff and can cause mechanical or thermal stress to components. Transfer molding is used to encapsulate some PBGA packages. Emerging for other PBGA applications is the use of liquid encapsulants. Liquid encapsulants are used where wire pitch is tight and for filling cavity packages. Liquid encapsulants are also formulated using epoxy resins, fused silica filler, and other additives. Being in liquid form, these encapsulant materials have low viscosity and can be filled with high levels of silica to impart desired mechanical properties. Liquid encapsulants are dispensed from a syringe. Depending on the PBGA configuration, a dam resin may be deposited as the first step. The dam resin defines the encapsulation area around the device. The cavity or defined

area is filled with encapsulant that covers the device and the wires. Finally a cure process is used. The lower viscosity of liquid encapsulants greatly diminishes the probability of wire sweep.

Terminals. There are two kind of interconnection terminals for BGA packages: ball and column (figure 3.2.27). The material is the standard lead-free alloy (SAC305, SAC 405) or special lead-free alloy (SAC387, SAC350, SAC266, a.s.o.), or SnPb for some applications.

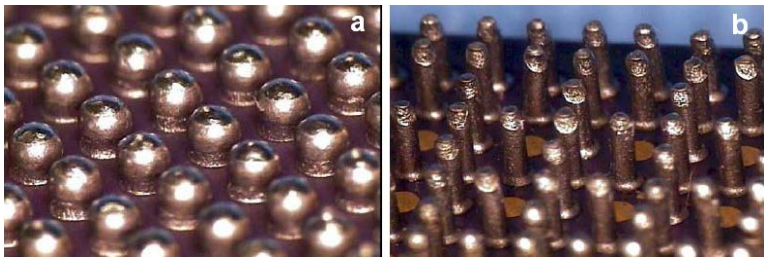


Fig. 3.2.27 Types of BGA terminals: a. Ball; b. Column

The µBGA package consists of the individual product die, a layer of compliant elastomer, and a flexible polyimide tape interconnect. Once the lead beams are bonded to the die, another layer of elastomer is added to protect the lead beams and die edges. The eutectic solder balls are then attached to the package lead beams. Because of the configuration of the flexible polyimide tape and the compliant elastomer material, the µBGA package exhibits improved coefficient of thermal expansion (CTE) compliant properties. Any associated lead beam stresses resulting from the CTE are dissipated via the elastomer encapsulation. A cross section of a µBGA is shown in figure 3.2.28. Micro-BGA package reliability is greatly dependent on the reflow soldering process. Many defects in BGA packaging arise from an inappropriate reflow profile. Researchers have been bringing forward various optimal strategies on reflow soldering to improve this packaging reliability.

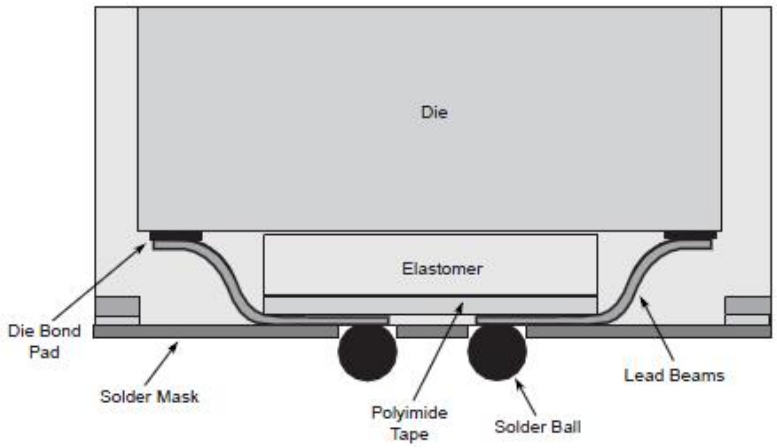


Fig. 3.2.28 A cross section of a µBGA (Intel)

Thermal performance of BGA packages

There are two thermal enhancements commonly employed in the design of an overmolded plastic BGA (PBGA) package, both illustrated in figure 3.2.29:

1) the addition of thermal vias and centrally-located thermal balls under the die;
2) the addition of metal planes in the package laminate.

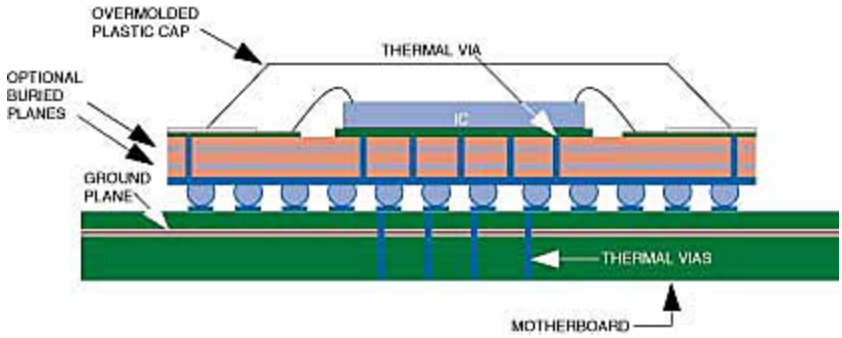


Fig. 3.2.29 Diagram of a PBGA package, soldered to a PCB

In the single-package test environment, it is customary to rate the thermal performance of a package by means of a thermal resistance value, called Q_{JA}. It represents the thermal resistance for the flow of heat between the junctions (the electrically active surface of the chip) to the air by all possible paths. Q_{JA} includes the contribution of the package, the PCB, and the heat exchange to the air. It is defined as:

$$Q_{JA} = (T_J - T_A)/P$$

where T_J is the junction temperature, T_A is the ambient air temperature, P is the total power dissipated by the chip. In SI units, Q_{JA} has units of °C/W.

The thermal performance of a standard PBGA package is compared to that of an otherwise identical package, containing one or both of these enhancements in figure 3.2.30. Each of these designs contains 352 peripheral balls. The designs with 36 thermal balls are described as 388 lead packages. Figure 3.2.31 illustrates the ball configurations for these packages. In the two-layer laminate configuration, the presence of the thermal balls produces a significant reduction in Q_{JA}. The best thermal performance, however, is provided by the configuration with the four-layer laminate.

The addition of thermal balls to the four-layer design provides only a minor improvement in the thermal performance.

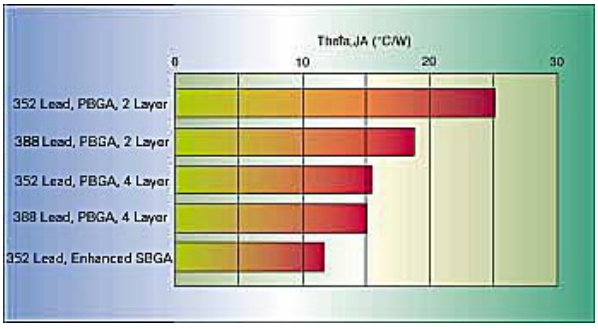


Fig. 3.2.30 Thermal performance comparison, various PBGA designs (35mm package)

The enhanced heat spreading afforded by the 4-layer design offers effective thermal coupling to all of the solder balls in the package. Hence, in this design, its thermal performance is only marginally affected by the addition of the thermal balls, representing less than 10% of the total number of balls. An alternative design, the SBGA package, which contains a copper-alloy heatspreader in a die-down design is also represented in figure 3.2.31. The direct attachment of the die to a copper-alloy heatspreader offers a level of thermal performance greater than that afforded by the PBGA designs considered here.

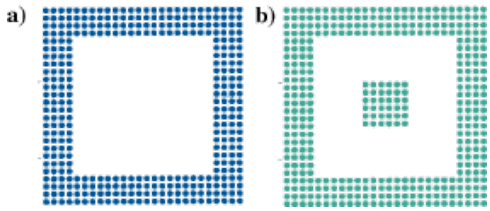


Fig. 3.2.31 Ball matrix configurations for (a) 352 lead and (b) 388 lead PBGA packages

Enhancement of the thermal performance of BGA packages is achieved using the same principle operative in the QFP designs: the reduction of the thermal resistance between the package and the board.

Power Distribution System

The evolution towards higher performance chips with increased transistor count demands improved power and heat dissipation requirements. AMITEC core-less substrate in FCBGA package format, is addressing this challenge by creating so called “Vertical Power Paths” (VPPs) through the entire substrate thickness (Z-axis). The thin film section in the AMITEC core-less substrate contains large amount of filled metal micro-vias that are redundantly distributed and vertically stacked to meet device pitch on one hand, and high current flow requirements on the other. When high current flows from the chip through the micro-vias, it will eventually hit the heavy copper planes or bus lines in the thick film section of the core-less substrate. In this section, large diameter and stacked copper pillars will further distribute the current outside the package. Needless to say, this path will also work the other way around, where high current is flowing into the low count yet large diameter copper pillars and then distribute to the thin film section by large amount yet small diameter filled micro-vias.

Types of BGA

Molded Array Process Ball Grid Array (MAPBGA). This wire-bonded type of BGA is an excellent package for low-performance to mid-performance devices that require packaging with low inductance, ease of surface mounting, low cost, small footprint and excellent package reliability. Features:

- Custom substrate designs/ball maps for maximum flexibility and electrical performance;
- Custom ball patterns/full array/depopulated arrays available; 0.5mm to 1.0mm pitch;
- Substrates use standard PCB manufacturing technology;
- Two- or four-layer substrates available (ground/power planes);
- High I/O with smaller footprints available;
- Maximum thickness from 1.00mm to 2.65mm;

- Capability to withstand lead-free reflow processes (260°C reflow).

Plastic Ball Grid Array (PBGA). The wire-bonded BGA package is a good option for mid- to high-performance devices requiring low inductance, ease of surface mounting, relatively low cost, and excellent package reliability. Additional copper layers in the substrate allow for increased power dissipation capability with the Thermally Enhanced PBGA (TEPBGA). Features:

- Custom substrate designs/ball maps for maximum routing flexibility and electrical performance;
- Custom ball patterns/full arrays/depopulated arrays available;
- Substrates use standard organic PCB manufacturing technology;
- Two or four layer substrates available (ground/power planes);
- Proven reliability in automotive/industrial environments;
- Capability to withstand lead-free reflow processes (260°C reflow).

Thermally Enhanced Plastic Ball Grid Array (TEBGA). In the TEBGA a thermally enhanced substrate acts to spread and draw heat from the die to the customer board. For further power dissipating capability, a heat spreader is placed on top of the die, within the mold compound of a PBGA, drawing heat to the surface of the package. Features:

- Builds upon the standard PBGA process;
- Overall substrate thickness increased over two-layer;
- Additional epoxy dispense, heat spreader placement, epoxy cure steps needed;
- Substrate design must account for heat spreader design to allow for attachment area;
- Proven reliability in industrial environments;
- Capability to withstand lead-free reflow processes (260°C reflow).

Tape Ball Grid Array (TBGA). The TBGA is a mid- to high-end BGA packaging solution for applications needing excellent thermal performance without an external heatsink. Features:

- Improved thermal performance over std PBGA packages <15°C/Watt;
- Custom substrate designs/ball maps for maximum flexibility and electrical performance;
- Custom ball patterns/depopulated arrays available; 1.0mm to 1.27mm pitch, up to 700+ I/O;
- Substrates use standard PCB manufacturing technology;
- Maximum thickness from 1.00mm to 1.65mm;
- Fine Lines/Spacing Geometry (35/35µm) on two sides of polyimide substrate;
- Capability to withstand lead-free reflow processes (260°C reflow).

Flip Chip Plastic Ball Grid Array (FCPBGA). This is a type of plastic BGA whose interconnect matrix uses Flip Chip packaging solution. Features:

- Improved board level solder joint reliability and lower cost compared to FC CBGA;
- Custom substrate designs/ball maps for maximum routing flexibility and electrical performance;
- Custom ball patterns / full arrays / depopulated arrays available, up to 800+ I/O;
- Substrates use standard organic PCB manufacturing and HDI laminate technologies;

- FCPBGA footprint is a drop-in replacement (PCB design and board assembly) for WB PBGA for the same ball diameter and pitch;
- RoHS compatible;
- Also available in a Land Grid Array format for reduced package profile.

3.2.9 System-in-Package (SiP) Technology

System-in-package technology builds on the innovative array interconnect of BGA and allows multiple die with complementary device technologies to be combined in a single package. Passive devices may also be included in the package to deliver highly functional integration for digital and radio frequency applications. Features:

- Flexible combinations of diverse device technologies;
- Highly compact compared to discrete solutions;
- Green (Halogen and Pb-free);
- Good thermal dissipation.

Design technology of SiP:

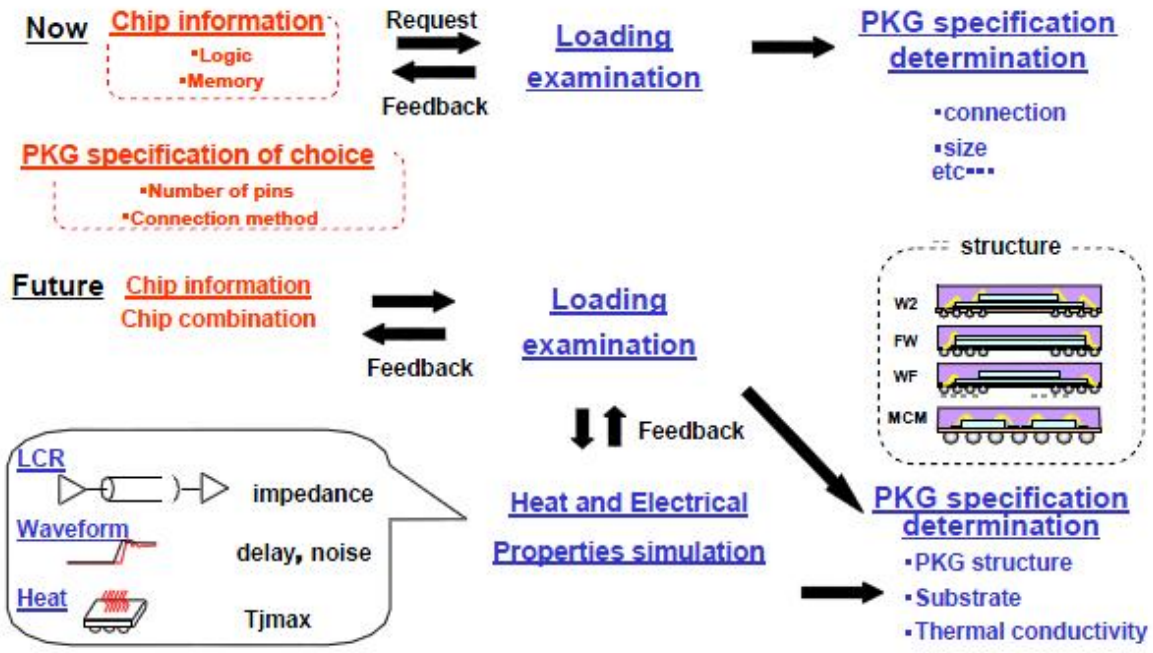


Fig. 3.2.32 Design technology of SiP

Key technologies of SiP:

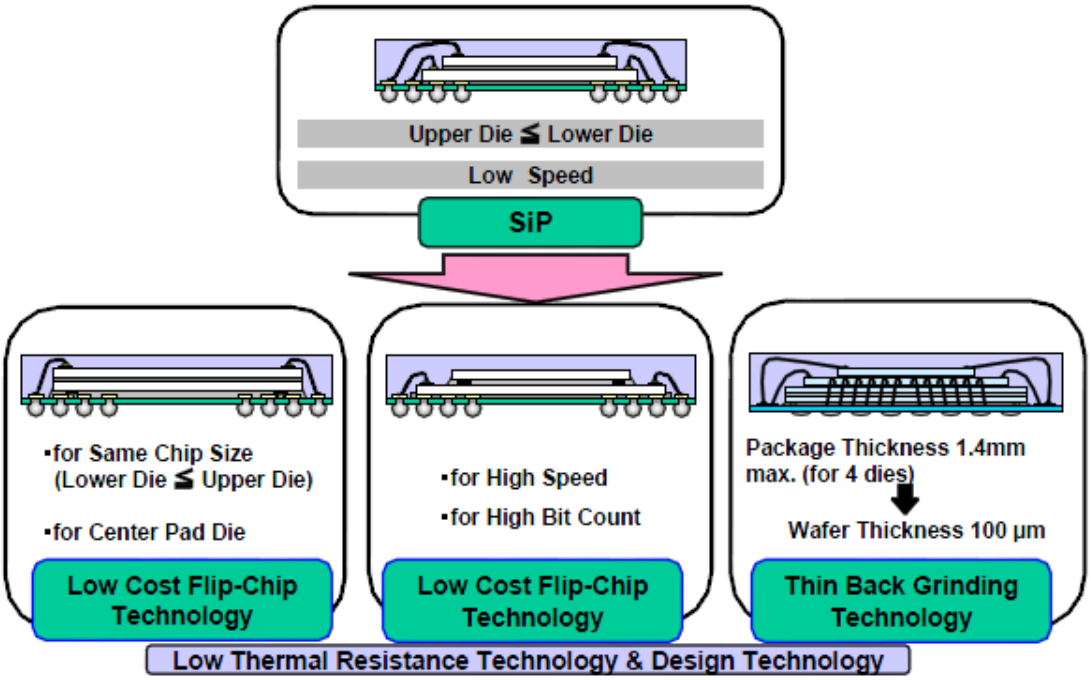


Fig. 3.2.33 Key technologies of SiP

Exemples of SiP:

System-in-Package Land Grid Array (SiP LGA). The System-in-Package Land Grid Array (SiP LGA) is a surface mounted plastic package with solderable interconnect lands on the bottom surface of the package. The SiP LGA is ideal for compact radio frequency (RF) applications in hand-held applications such as transceivers, power amplifiers, and front end modules. Features:

- May include multiple die;
- May include passive devices (filters, crystals, capacitors, inductors, resistors);
- Substrate uses HDI laminate technology;
- Uses lead-free and halogen-free packaging materials;
- Uses high-thermal conductivity die attach material for power amplifier applications;
- Maximum package thickness of 1.10 to 1.60mm;
- Production qualified to MSL3, 260ºC reflow.

Stacked Die System-in-Package. The stacked die SiP package offers flexibility in combining die from different fab processes into a single package. Board area savings are realized by stacking the die vertically vs a side by side approach. This package technology is mainly used where X-Y size constraint is the critical requirement. Features:

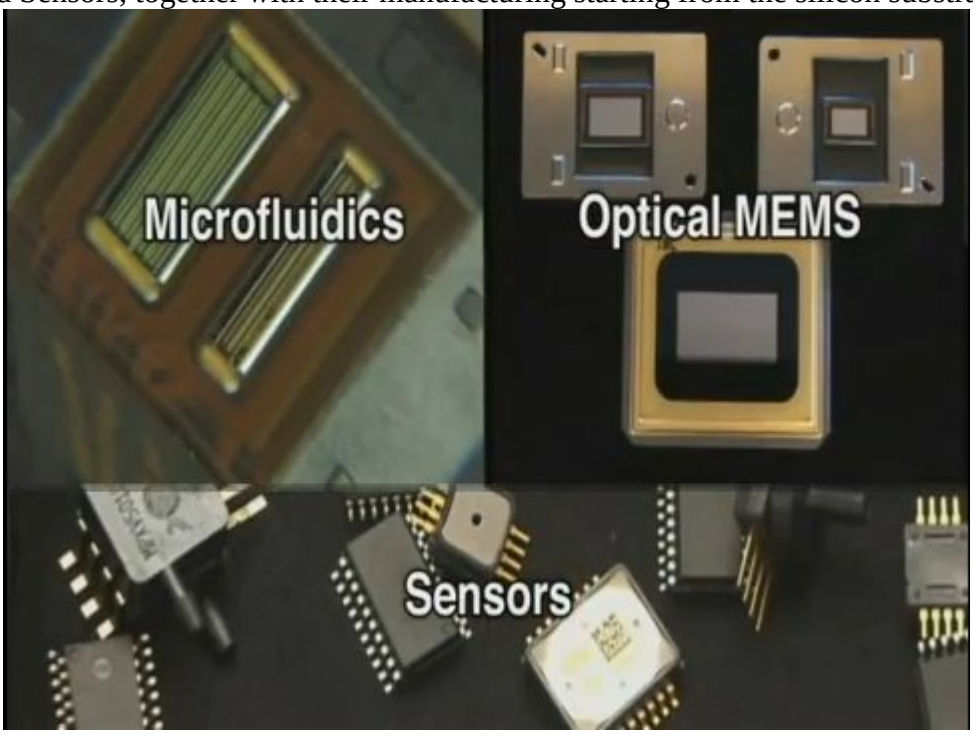
- Includes multiple die (ranging from 2-4 separate die);
- Uses lead-free and halogen-free packaging materials;
- Maximum package thickness of 1.2mm – 1.6mm;
- May include baseband and memory or baseband and RF die;

- Production qualified to MSL3, 250ºC reflow.

Package-on-Package (PoP); System-in-Package. The PoP package allows for stacking a memory package on top of the baseband device. The baseband package has perimeter lands on the top surface of the package to facilitate package stacking. This technology allows the baseband and memory devices to be tested separately prior to assembly. Features:

- Substrate utilizes HDI laminate technology;
- Uses lead-free and halogen-free packaging materials;
- Maximum package thickness of 0.9mm;
- Top surface solder lands to accept JEDEC standard Memory PoP packages;
- Production qualified to MSL3, 260ºC reflow.

The documentation film from below presents in a few frames the Microfluidics, Optical MEMS and Sensors, together with their manufacturing starting from the silicon substrate.



Micro-machines for making MEMS
(http://www.youtube.com/watch?v=_GOfdHMA4to&feature=related)

3.2.10 Multi-Chip Modules (MCM)

Basics

Multichip packaging is being developed to meet the demands for higher performance and further miniaturization. There are many factors to consider during the design stages of circuit board manufacturing, and speed and size are among them. Moreover, manufacturers want to minimise size and maximise speed without incurring additional costs. These design developments apply array technologies, SMT, and a variety of plastic, ceramic and thin-film

materials. Multi-Chip Modules (MCMs) represent a technology that meets such needs. MCM packaging is an important facet of modern electronic miniaturization and micro-electronic systems. The modules consist of two or more chips, mounted by wire-bonding, flip-chip, or tape automated bonding onto a second-level package that is then placed onto the board. Within the module are various types of connection – between the elements of the module, or between the elements and the substrate. The second-level package may also contain plated through-holes and vias, and is attached to the board by pin, pad or solder bumps. The substrate is an important part of the package, providing mechanical support, electrical conductivity or insulation and/or thermal conduction. Substrates can be routable or non-routable, but most MCMs are routable. As such they give signal, power and ground routing, whereas non-routable substrates act as heat sinks. A MCM is a specialized electronic package where multiple integrated circuits, semiconductor dies or other modules are packaged in such a way as to facilitate their use as a single IC, thus the MCM is referred to as a "chip" in designs.

There is a classification of MCMs according to the technology used to create the HDI substrate (figure 3.2.34):

- ♦ MCM-L - Laminated MCM; the substrate is an organic laminate multilayer board structure, similar to standard printed wiring boards (PWBs), but with denser component placement and greater wiring densities;
- ♦ MCM-D - Deposited MCM; the modules are deposited on the base substrate using thin-film structures on semiconductor or ceramic base layers, with deposited metal conductors and dielectrics;
- ♦ MCM-C - thick-film or cofired Multilayer Ceramic technology, such as LTCC.

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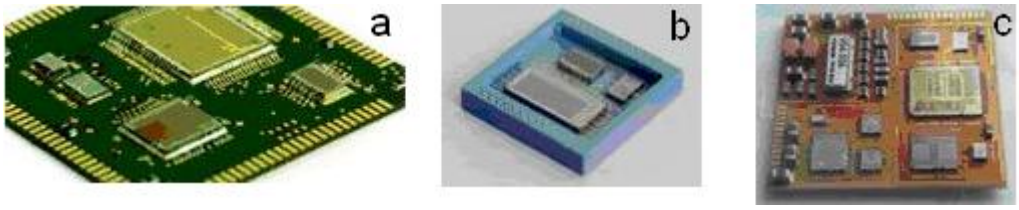

Fig. 3.2.34 Multi Chip Modules: a) MCM-L; b) MCM-C; c) MCM-D

The MCM was developed in the early 1980s and is an evolution of the traditional hybrid package that appeared soon after the birth of the IC. Today's high-performance supercomputers and mainframes require many, many chips to form one central processing unit (CPU), in contrast to today's personal computers (PCs) that typically use one chip for each processor. MCM technology allows chips to be spaced more closely with less overall volume and weight than individually (single chip packaging) packaged parts. Since MCM packages are very dense with minimum volume and weight, they have widespread application in aerospace, medical, consumer, and all portable products in addition to supercomputers and mainframes.

Clearly, the MCM, by its very nature-multiple chips on a substrate or carrier-is different from its individually packaged counterpart. What sets it apart from its precursor, the hybrid, is the chip density. It is commonly held that for a package containing multiple chips to be classified as an MCM, 50% or greater of the substrate (carrier) or packaging area must be covered with active semiconductor devices.

The substrate or carrier is the key element in any MCP and especially in the MCM. The substrate provides the mechanical attachment for the chips, handles the interchip signals, provides power and ground for all chips, and interfaces the module with the next level system elements. In addition, the substrate can play a major role in module thermal management, as well as help protect the chips from environmental impact.

Multi-chip Module Functionality

As schematically illustrated in the figure 3.2.35, the MCM provides the circuit designer and packaging engineer with a highly functional building block for the implementation of complex circuits, subsystems, and even small systems in certain applications.

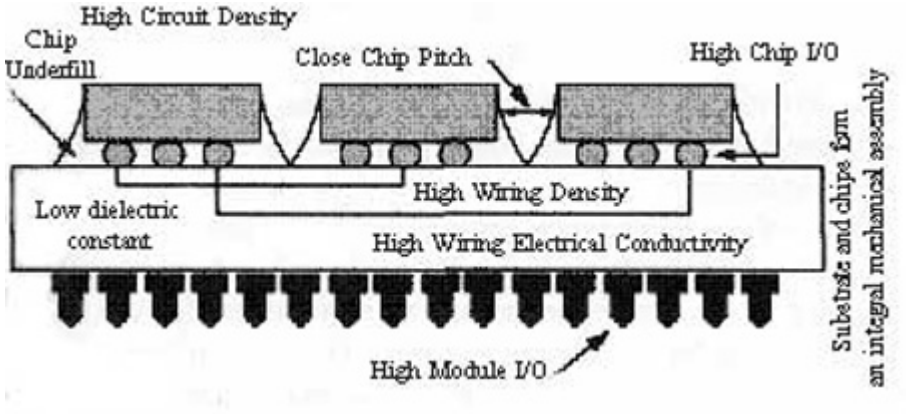

Fig. 3.2.35 Multi Chip Module structure

To be a highly functional MCM, the following criteria must be satisfied:

- Chip-to-chip spacing in the MCM must be held to a minimum to minimize signal propagation delays. Close chip spacing requires the substrate to have high density wiring to support the I/O requirements of each chip without an undue size or layer penalty. Because of their small size, conductors must be made of high conductivity metals to avoid excessive lead resistance. In addition, the traces must be properly designed to prevent signal distortion and minimize crosstalk and noise.
- The MCM must provide a means of thermal management to limit the junction temperature of the semiconductor chips to temperatures less than 85-100°C. Thermal management is typically accomplished through substrate conduction of the heat when chips are mounted to the substrate in the face-up configuration. If chips are flip-chipped-mounted in a face-down configuration-as shown in figure 3.2.30, then thermal management can either be accomplished through the leads (solder balls) in low power applications or by the use of thermally conductive fingers for heat removal in high power applications.
- The MCM must provide reliable I/O connections to the next level of assembly in the system. Typically, this takes the form of an interface with a PWB, although direct module interface with external system elements is possible. The number of module I/O is significantly reduced from the sum of the module's individual die or chip I/O numbers. If the MCM doesn't reduce overall I/O, then the partitioning of the circuit, or the overall

requirement for the MCM, must be questioned. A method for calculating module I/O based on the constituent chips and their respective I/O is called Rent's Rule.

- The MCM must provide protection from the environment. Some technique for sealing the packages, or at least overcoating/encapsulation of the chips and their interconnects, must be provided.

Multichip Module Advantages and Efficiency

One way of distinguishing an MCM from other single and MCP styles is to consider its packaging efficiency. Packaging efficiency is defined as the ratio of the area of all the base chips to the area of the MCM substrate or, for individually packages parts, the area of the system-level board. Single chip packages such as dual-in-lines (DIPs) or quad flat packages (QFPs) require a lot of board real estate due to the packaging size itself and the need to have peripheral leads. The board-level efficiency with such packages (DIPs, QFPs) is quite low, typically around 10%. Even with standard ball grid arrays and chip scale packages, the packaging efficiency rarely approaches 50%.

As shown in the figure 3.2.36, the packaging efficiency of MCMs varies widely, approaching 80%, with laminate and ceramic MCMs providing the lowest and thin-film multilayers providing the highest. This packaging efficiency is directly proportional to component I/O and the wiring density supported by the substrate. Thin-film MCMs possess the highest wiring density, measured as length of minimum width track possible per unit area, and typically provide the highest packaging efficiency because they can interconnect the ICs in the smallest area. Small-area, high-density packages such as MCM-Ds offer significant benefits in addition to size, including better electrical performance due to shorter wiring length, and improved reliability due to elimination of one level of interconnect.

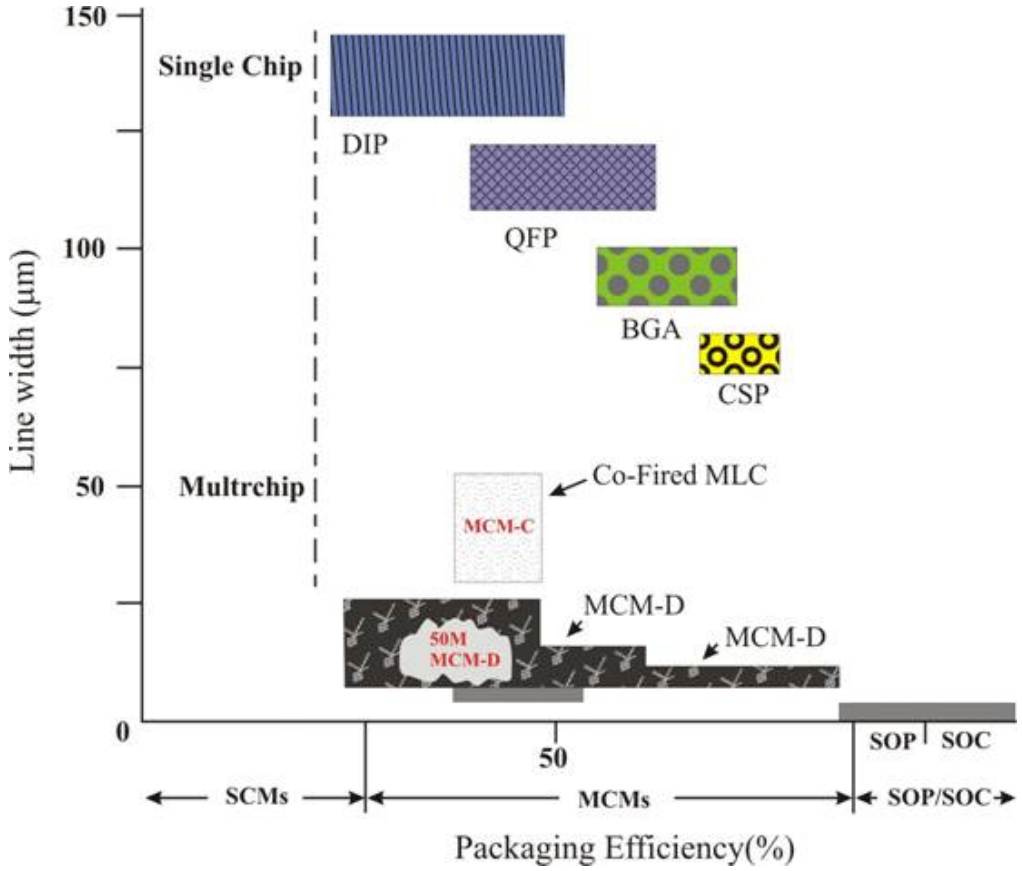

Fig. 3.2.36 Packaging efficiency vs. Line width for different packages

The need for the MCM arises because the circuit designer cannot obtain enough functionality in a single chip. As the march of integrated technology continues rapidly, it ultimately may be possible to have the entire system function on a large single chip or wafer. This wafer scale integration (WSI) holds the prospect of going back to single chip packaging techniques, but until it is a practical reality, multichip packaging will be required. In fact, MCP will always be used to address special circuit needs and the requirement for system redundancy. Thus, in today's electronic packaging world, there appear to be three major options for system-level packaging:

- WSI with the system on a single chip (system-on-chip [SOC]);
- MCMs formed from multiple chips on a common substrate/package structure;
- Individually packaged chips on a PWB.

It should also be noted that if all the functionality that could be packaged in an MCM was integrated into a single chip, the chip would become very large and the device feature size extremely small. This would result in very complex technical requirements and, hence, high development and manufacturing costs. Since the MCMs use less complex chips and, for the most part, can be repaired, they can be less expensive, and easier and faster to develop. Thus, until WSI (SOC) can be performed with high yield and relatively low development costs, the MCM will be the high performance (speed, volume, weight) mainstay for system packaging.

MCMs have four major advantages over individually packaged parts:

- higher packaging efficiency (area of chip to area of the board), due to the fact that the bare chips can be placed much closer together than the chips in single chip packages (because of the wasted space of the packages themselves);
- better electrical performance due to the shorter distances between chips and, hence, reduced substrate wiring length as well;
- greater reliability due to reduced number of interconnects between the chip and the board (the MCM eliminates one level of interconnect;
- the MCM (in high volume) offers the potential for lower cost because of the elimination of the individual IC packages and the reduced substrate size.

Organic substrates-based: Multi-Chip Module – Laminate (MCM-L)

Basics

MCM-L technology is a laminate construction and is basically a further development of PCB technology with two or more bare chips and fine line interconnects in order to accomplish the denser integration requirements of today's demands. Consequently, it is perceived that the current PCB fabricators are ideally positioned to take the initiative with MCM-L technology. Thus, MCM-L became the fastest growing component of overall MCM sales.

A significant factor in MCM-L development was the introduction of low-melt flip-chip processes. Flip-chip die can now be connected to laminate carriers using slightly modified surface mount processes. Advances in laminate structures, such as high-density Microvia substrates, have accommodated line widths and spacings down to 50µm and vias down to 90µm. This is significant for enabling the escape of the dense I/O grid of flip-chip die. The smaller vias and fine lines allow more signal lines to be routed between the pads, thereby reducing the overall number of layers required. Advancements in moisture sensitivity coupled with new underfill formulations have lead to robust designs. These designs can withstand factory conditions of 30ºC and 60% relative humidity for up to one week and suffer no adverse effects during the subsequent second-level assembly processes.

Comparison with MCM-C and MCM-D:

- ♦ Low cost;
- ♦ Parallel fabrication process;
- ♦ Ease of repairing of reworking individual layers;
- ♦ Well established infrastructure;
- ♦ Assemblies with components in both sides;
- ♦ Significant CTE mismatch between substrate and die materials;
- ♦ Low performance and wiring density;
- ♦ Poor thermal conductivity of substrate;
- ♦ Moisture sensitivity of materials;
- ♦ High Crosstalk noise.

A cross section of a MCM-L is shown in figure 3.2.37. Improved or high end PCB technology for MCM-L applications comprises new or improved PCB base materials (FR4, FR5, BT, etc), improved solder masks materials, surface finish for bondability, flip chip, smaller

mechanical drill sizes or laser drilled, thin dielectric layers (down to 50µm), small lines and spaces (down to 75µm), additional distribution layers (polyimide, epoxy, etc).

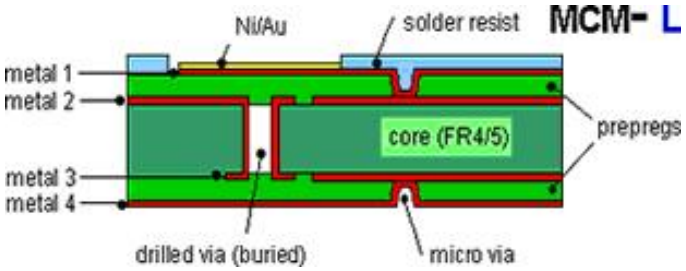

Fig. 3.2.37 MCM-L cross-section

The MCM-L technology is not always the best solution, especially with respect to long term reliability.

Sequential Build Up Process (SBU)

The additive process of the SBU technology avoids the limitations inherent in the subtractive process that is used with the traditional laminates (pre laminated with copper foils). There is either any need for all the process chemistry involved in the plating of high aspect ratio through-holes in the traditional process. There are different process steps.

Via holes. The main limitation to increased density of conventional circuit boards is area needed for via generation. In the SBU techniques, both the hole diameter as well as the annular ring diameter may be significantly smaller. The reduction in hole diameter is partly because of the thin dielectric layer and the hole forming techniques. The latter because there will be no miss-registration as it is with the conventional stacking of prepregs. A 250µm drilled hole in a multilayer board will typically require a 625µm via pad with a minimum hole to hole pitch of 750µm. For SBU technology an inner layer hole diameter of less than 50µm is currently in production.

Three different techniques are used for creating the via-holes:

- photo-defined vias;
- laser-drilled vias;
- plasma-etch vias.

A cross section of a metalized laser-drilled via is shown in figure 3.2.38.

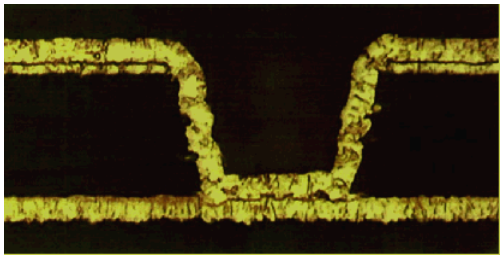

Fig. 3.2.38 Cross section of metalized laser-drilled via

Flexible base material. Conventional flexible base materials are made by bonding the copper layer to the polyimide dielectrics with an adhesive. However, the use of an adhesive layer increases the z-axis thermal expansion of the laminate which can cause cracking of the through hole metallisation during thermal cycling. Eliminating the adhesive using adhesive-less flexible base material is the best way to minimise the cracking tendency. This can be obtained in three ways:

- Chemical deposition*;*
- Vacuum deposition;
- Casting.

Wire bonding on SBU. Wire bonding typically requires between 100 and 1250nm of soft gold on the bond pad. For thin layers (100 – 200nm) immersion gold can be used. This process is self-limiting, and gold is plated on all exposed surfaces, after the solder mask has been applied. Once a complete gold coverage of the surface is achieved, the plating process stops. Immersion gold is the least expensive gold finish available. This coating is commonly used for ordinary surface mount assembly, and provides excellent solderability and coplanarity without a significant cost increase compared to other finishes. This means that the same finish can be used for both wire-bonding and soldering. If higher gold thickness is needed (500 – 1000nm) for gold wire bonding, electroless gold can be used. The electroless process means that all exposed metal surfaces will be plated. The process will continue as long as it immersed into the plating bath. However, this amount of gold will have a negative effect on the solder, causing a brittle joint. If thicker gold is needed, electroplating has to be used. Electroplated gold is selectively added onto the metal surfaces that are included in the external electrical circuit. This means that all wire bonding pads must be connected together in a bus. The electroplating is a more costly process, and the required bussing can cause some design (layout) problems.

The gold thickness influences on the wire bond pull strength.

During the bonding process, under pressure and high temperature above the glass transition temperature the PCB will deform under the bond area often called cupping. This cupping effect will dissipate the ultrasonic energy, reducing the bond yield. However below T_g, the PCB is hard and rigid and gives few problems in the wire bonding process. The use of nickel under the gold finish increases the stiffness of the pad. In addition, the nickel acts as a diffusion barrier between the copper and gold. If the gold thickness is more than 1.25mm, there is no need for the diffusion barrier. Other options to increase the stiffness and hardness are to use thin coatings of tungsten or titanium (30-50nm). Higher T_g materials allows increased bond temperature (increased ultrasonic energy) without exceeding the glass transition temperature. Also a larger bonding pad will help dissipate the heat from the bond area and therefore reduce the localised temperature of the substrate under the bonding pad. The use of thinner wires will allow bonding with lower pressure and reduced cupping effect.

Dielectrics for SBU. The dielectric material used in sequential build up technology has to fulfil several requirements. These are:

- Provide a suitable surface for metal plating, with good adhesion and stress compliance;
- Good adherence to different substrate materials;
- Simple processing;

- Good dielectric properties (low dielectric constant and low dielectric loss);
- Low moisture absorption;
- Allow deposition with a well controlled thickness onto the substrate;
- Glass transition temperature above 150 ^{o}C;
- Low thermal expansion coefficient.

As dielectrics used in SBU technology are: epoxy, acrylate, polyimide.

The dielectric can be applied to the substrate in different ways:

- by moving the substrate on a conveyor through a sprayed "curtain" of the dielectric: this method gives high transfer efficiency, however the thin layer of dielectric falling through the air gives a significant loss of solvent; typically, thickness in the 25 to 60mm can be obtained in this way;
- spin coating: this gives thinner layers, less than 20mm; the transfer efficiency is however low; nevertheless, this is the method of choice for high cost polyimide solutions, since the equipment is well characterised from the semiconductor industry;
- spray coating: this has a potential efficiency in between curtain and spin coating; with a proper design of the equipment and the use of low pressure high volume spray, good coatings can be obtained; there is neither a need for high solvent dilution;
- roller coating: both sides of the substrate can be coated in the same process.
- dry films dielectric: this has significant drawbacks as poor conformity to varied surface topography, loss of possibility of customised thickness and high cost;
- photoimageable dielectrics causes a significant reduction in the number of process steps; the result is also less waste and increased throughput.

Metallisation. The conventional metallisation process is based on electroless copper plating. A temporary plating resist is used to define the conductor tracks. Often a "swell and etch" adhesion promotion system is used to increase the adhesion between metal and polymer as well as increase the ability to comply with mechanical stress. A palladium/tin colloidal is typically used as a catalyst for the deposition of copper. With electroless process, the plating can be done on many panels in a batch process. The plating is uniform, and it will conform to the substrate and provide a coplanar surface regardless of the topography or features.
Adhesion to the substrate is often measured by a peel testing, where the metal is peeled normal to the substrate.

Case study

C40 Processor MCM for Digital Signal Processing. A miniaturised general-purpose DSP MCM, which takes up 6x less area than the conventional SMT approach, has been developed by GEC-Marconi (figure 3.2.39). Featuring Texas Instruments C40 DSP processor, 384Kx8 SRAM, dual port RAM (2Kx16 for interface), decoupling capacitor included, and the module was fabricated on organic substrate (MCM-L) technology. MCM-L was chosen because it offered the optimum combination of size reduction, very good electrical properties, low weight and an easy way to incorporate thermal vias and a metal core, to extract heat. The IC connections were made by wire-bonding, which enabled standard ICs to be procured easily while still providing a substantial reduction compared to SMT. A metal package was chosen for hermeticity and

electrical screening reasons. The module has the dimensions 50x50mm, 5 layers, 75µm tracks, gaps and vias, thermal vias and metal core to aid thermal management, 160 I/Os.

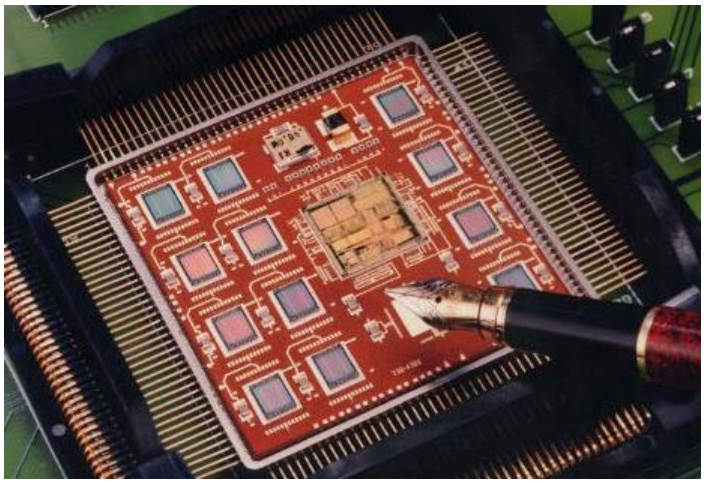

Fig. 3.2.39 C40 Processor MCM-L (GEC-Marconi)

Ceramic substrate-based: Multi-Chip Module – Ceramic (MCM-C)

Basics

Clearly the infrastructure for ceramic MCMs has been in place long before laminates. In the mid-1970s, ceramic MCMs were capable of integrating over 100 chips on a single substrate. Figure 3.2.40 illustrates an example MCM-C configuration with the parts and processes that are available. The MCM-C technology is used to manufacture microcircuits for electronic systems that require increased performance, reduced volume, and higher density that cannot be achieved by the standard hybrid microcircuit or printed wiring board technologies.

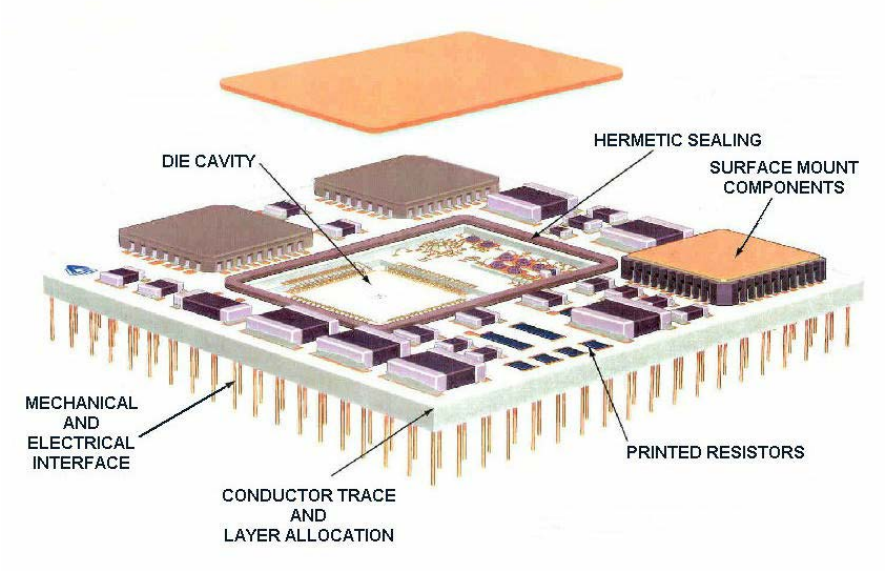

Fig. 3.2.40 A MCM-C configuration

Materials

Substrates. Important properties of thickfilm substrate materials are:

- ♦ Good dimensional stability during high temperature processing;
- ♦ Good adhesion between substrate and printed materials;
- ♦ High thermal conductivity;
- ♦ A thermal coefficient of expansion matching that of other materials in the circuit;
- ♦ High electrical resistivity that gives isolation between components;
- ♦ Low dielectric constant;
- ♦ Low dielectric loss tangent (for microwave circuits);
- ♦ Good machinability;
- ♦ Low price.

In order to satisfy all the necessary requirements various types of ceramic are used as thick film substrate materials, with 96 % Al_2O_3 (alumina) as the dominant one.

Alumina has many good electrical and mechanical properties, as well as very good dimensional stability. It is brittle, and this limits the maximum size to 10 - 15cm. After the material has been sintered, it is not easy to shape it. However, it can easily be cut by breaking after a partial cut is made by a high power laser, or after tracing with a diamond. For small circuits, it is common to print and mount components on many substrates that are produced together and then broken apart in the end, to make a rational production process. Holes through the substrate may also be made by laser, but it is simpler to form the substrate contour and punch holes while the ceramic is pliable, before the sintering. The thermal conductivity of 20 - 30W/ºC is approximately 100 times better than for organic materials, and the low thermal coefficient of expansion, 6ppm/ºC, is advantageous for the mounting of ceramic components and semiconductor chips.

Aluminium nitride (AlN) substrates are used today for circuits with very high power dissipation. AlN has 5 times or higher thermal conductivity than Al_2O_3. Many properties are similar to those of Al_2O_3. The thermal coefficient of expansion is somewhat lower, 4.5ppm/ºC. This, and different surface properties, give a need for special printing pastes on AlN, to avoid flaking off during the high temperature processing.

BeO has even higher thermal conductivity than AlN. However, its use is limited by the fact that dust and vapour from BeO are very poisonous. High price is also connected to this fact.

Enamel coated metal is used as substrate for high volume products with lower electrical demands, to some extent.

Conductors, resistors and dielectric materials are applied in paste form by screen printing and they are transformed/sintered by heating to high temperature, "firing". The pastes have three main ingredients:

- ♦ Functional element (metal-, alloy- or oxide particles);
- ♦ Matrix or "binder" (glass particles);
- ♦ Organic solvents and "temporary binder".

The organic, temporary binders are polymers that give control over the printing properties. They decompose and evaporate early in the firing process, together with the solvents. The glass particles melt in the firing process, adhere to the substrate, bind the active particles together and give stability for the circuit. The high firing temperature is typically 800 - 900ºC. The conducting pastes should give:

- ♦ High electrical conductivity;
- ♦ Strong adhesion to the substrate;
- ♦ Excellent solderability for soldering of packaged components;
- ♦ Reliable bondability for wire bonding of naked IC chips;
- ♦ Price is also an important parameter.

Normally one conductor paste cannot satisfy all these criteria, and it is necessary to make several conductor prints. The most used conductor systems are gold, copper, alloys of palladium/silver, palladium/gold and platinum/gold. Noble metal systems are used because the heat treatment takes place at above 800ºC, where other metals are ruined by oxidation. However, gold and platinum are expensive materials, so the material cost is an important factor in the final price of the circuit. Gold is very well suited as basis for bonding, but it is not suitable for soldering. This is because gold is very quickly dissolved in solder metal during the soldering process, and it gives a brittle inter-metallic composition with poor reliability properties. Pure silver has a strong tendency for migration, which may cause reliability problems after some time. However, silver/palladium gives little migration, it is excellent for soldering, and is well suited for making contact areas for printed thick film resistors. Therefore, this alloy is the most used as conductor material, although it has lower conductivity than the pure elemental conductors. Silver is also used in alloys with platinum.

Copper has high conductivity and low price. However, strong oxidation in air at high temperature makes it necessary that copper must be fired in a neutral nitrogen atmosphere. This process is more complicated and costly and has impeded the use of copper conductors.

Nickel is also used to some extent, but it has lower electrical conductivity than the other materials.

Silver with 1% platinum (AgPt) has similar leach resistance and migration properties as AgPd, but the electrical conductivity is much higher. Gold – platinum is sometimes used, since has excellent soldering properties.

Typical thickness for the conductors is 5 -10µm after firing.

Resistors. Important properties of thick film resistors are:

- ♦ Large range of available resistor values;
- ♦ High stability;
- ♦ Low thermal coefficient of resistivity, with little spread over the substrate;
- ♦ Low voltage dependence of the resistance;
- ♦ Good noise properties.

The resistor pastes consist of the same three main ingredients as the conductor pastes, but the active elements have lower electrical conductivity. They are most often based on various types of oxides of ruthenium: RuO_2, $BaRuO_3$, $Bi_2Ru_2O_7$. In addition, oxides of iridium, rhodium and osmium are used. They may be produced with sheet resistance down to approximately 1 ohm/sq, and up to 109 ohm/sq, for a 25 µm thick print. The sheet resistivity is determined by the active material in the paste, the amount of glass matrix mixed in, and the details in the processing. The tolerance in achieved resistance is lowest for the intermediate values of sheet resistivity. Resistance drift lower than 0.5 % under harsh climatic conditions over long periods of time makes thick film hybrid technology attractive for demanding applications. The difference in drift between several resistors on the same substrate is typically 0.1%. The temperature coefficient of resistance depends on the material, and it is typically in the range +/- 100 - 700 ppm/ºC, with variation over a circuit, for resistors printed with the same paste, below +/- 15 ppm/ºC. The tolerance in absolute resistance after printing and firing is typically +/- 10 - 20%, and the relative tolerance between resistors on the same substrate one order of magnitude lower. However, by laser trimming one can achieve tolerances down to approximately 0.5% absolute, and 0.1% relative value.

Dielectric materials are printed to obtain insulation between various layers of conductors, to produce capacitors, and as passivating cover on top of the whole circuit. For insulation, low capacitance between conductors is desirable and we use materials with low dielectric constant. For capacitors, materials with high dielectric constant are used, to achieve high capacitance with little area consumption. Important properties of dielectric materials are:

- ♦ High insulation resistance;
- ♦ High breakdown field;
- ♦ Low loss tangent;
- ♦ Low porosity.

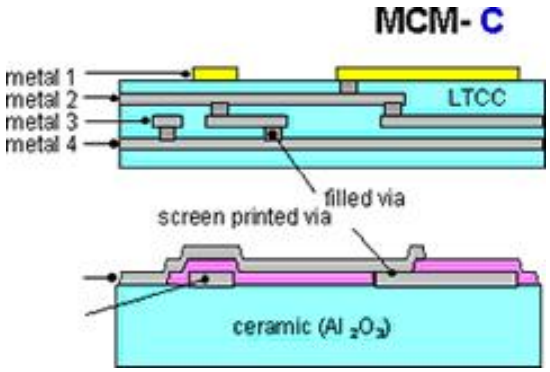

Fig. 3.2.41 MCM-C cross section

Also, for insulators low dielectric constant is a must, and for capacitors, suitable dielectric constant, low temperature coefficient and low voltage coefficient of dielectric properties are important too. For insulation layers, aluminium oxide is the common functional element, together with glass. The glass melts and crystallises during firing at 850 - 950ºC, but it does not melt if heated again. The relative dielectric constant is typically ε_r = 9-10, and breakdown field strength 20V/µm. The dielectrics for high value capacitors consist of ferroelectric materials with ε_r up to above 1000, similarly to ceramic multilayer capacitors. However, the properties of these materials change drastically near the Curie temperature. Barium titanate is used, with additives

of strontium, calcium, tin or oxides of zirconium to change the Curie temperature and to reduce the temperature coefficient in the temperature range of use. That gives ε_r = 1000 - 3000 and temperature coefficient up to approximately +/- 5000ppm/ºC. For small capacitors the pastes of magnesium titanate, zinc titanate, titanium oxide, and calcium titanate are used, with ε_r = 12 - 160, and temperature coefficient +/- 200ppm/ºC. Capacitors are not suitable for laser trimming, therefore. Printed capacitors are used only in small values and for uncritical purposes (de-coupling capacitors, etc.).

A cross section of a MCM-C is shown in figure 4.2.41.

Processes

There are two different processes in MCM-C categories:

- several conductive layers deposited on a ceramic substrate and embedded in glass layers;
- several conductive and ceramic layers co-fired at high (HTCC) or low (LTCC) temperature.

The state-of-the-art is demonstrated by four different processes:

- Standard process;
- Fine line;
- Photo-imageable;
- Low Temperature Co-fired Ceramic (LTCC).

Trimmed precision resistors are available for each process (range: 1Ω to 10ΩM). The differences between first three processes are in the width and the line to line pitch of conductors (they decrease from 254µm to 75µm). The standard process is qualified for space environment; all processes are qualified for all other environments (industrial, automotive, military). All processes are used for all applications: analog, digital, mixed, microwaves.

Comparison with MCM-L and MCM-D:

- High wiring density
- Better electrical and thermal conductivity than MCM-L
- Assemblies with components on both sides
- Flexible packaging
- Superior strength and rigidity
- Parallel manufacture process
- Lower wiring density than MCM-D
- High dielectric constant (not suitable for high frequencies)
- CTE mismatch between substrates and die materials

Silicon substrate-based: Multi-Chip Module – Deposited (MCM-D)

Basics

MCM-D (figure 3.2.42) are formed by using thin-film deposited as dielectric and metallisation, formed on dimensionally stable bases. The photolithography process used to apply and pattern the dielectric and metallization are the ones commonly used in the semiconductor industry. The metallization layers consisting of power planes, signal layers and die bonding pads are done by conventional sputtering, vacuum evaporation methods or electroplating followed by

normal photolithography steps. Wet etching, plasma etching or lasers are normally used for processing vias. Additional layers may be added to include thin-film integrated resistors and thin-film capacitors as an option. A future possibility will be to incorporate additional circuitry such as memory, module input/output protection (ESD, EMC) in the bulk substrate if silicon is used for the substrate. This implies a better utilisation of the active silicon area because the I/Os on the chips can be considerably simplified and thereby require less space. Comparison with MCM-L and MCM-C:

- ♦ Highest performance
- ♦ Highest wiring density
- ♦ Low dielectric constant
- ♦ Good electrical properties
- ♦ Highest costs

Materials

The base materials for MCM-D are silicon, aluminium, alumina ceramic or aluminium nitride.

The metal used for most thin film conductors is gold, because it is chemically stable, it has high electrical conductivity and good bondability. However, gold diffuses very rapidly into many other metals. Together with gold, special elements are used as diffusion barriers and in addition as adhesion layers, because gold has poor adhesion to non-metallic materials. Nickel is suitable for diffusion barrier, a nickel/chromium alloy improves the adhesion, and it is also suitable as resistor material. The much used Au - NiCr system is deposited by vacuum evaporation or by sputtering. Gold may also be electrolytically plated. This is particularly important for microwave circuits, where a 5 - 10µm thick layer gives low conductor resistance, reducing the high frequency loss.

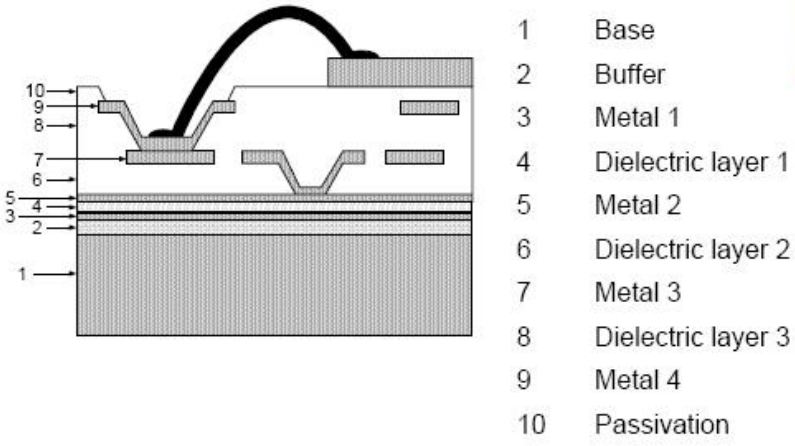

Fig. 3.2.42 MCM-D cross section

Various materials are used for dielectric depending on the aim: to make capacitors, multilayer insulation or passivation. For passivation, SiN_3 is well suited. SiO_2 is used much for insulation between conductor layers, because it has low dielectric constant ($\varepsilon_r = 4$), and high breakdown field strength (10^6V/cm). Both are produced by chemical vapour-phase deposition.

For capacitor dielectric SiO_2, Al_2O_3, Ta_2O_5 are used. They are produced by vacuum evaporation, chemical deposition, or anodic oxidation.

Resistors are made, as mentioned, from NiCr, as well as Ta_2N, by vacuum evaporation or by sputtering.

Processes

The process steps for a thin film circuit, with one conductor layer and one resistor layer is presented in figure 3.2.43. In the first step, the resistor layer is deposited all over the substrate. If the circuits are small, many circuits are made on the same substrate, and they are separated at the end of the production process. First a diffusion barrier (also improves the adhesion) is deposited and then the conductor metal. This is preferably done in the same vacuum chamber, in order to have a clean surface and good adhesion. These standard processes require special equipment and clean room facilities. Minor thin film circuit producer companies will normally buy the substrates, which are processed to this stage.

Conductor and resistor geometries are defined by photolithography and etching. A few drops of photo resist are deposited and spread by the centrifugal force when the substrate is rotated on a spinning disk. The conductor pattern for the circuit is defined by exposing the resist through a photo mask, development and curing. Then the gold is removed by etching where it is not wanted. A solution of potassium iodide solution may be used for etching the gold, without dissolving the NiCr layer. If the need exists for conductor widths less than 2-3µm, the etching is done by reactive ion etching, which etches fast vertically, but more slowly horizontally, and thus reducing the under-etching. A new step of photo-processing is done to define the pattern of the resistors, and the diffusion barrier and the resistor films are etched where they are to be removed, for example with nitric acid. (Where the circuit has conductor pattern, there is still the resistor layer underneath the conductor material, see figure 3.2.43).

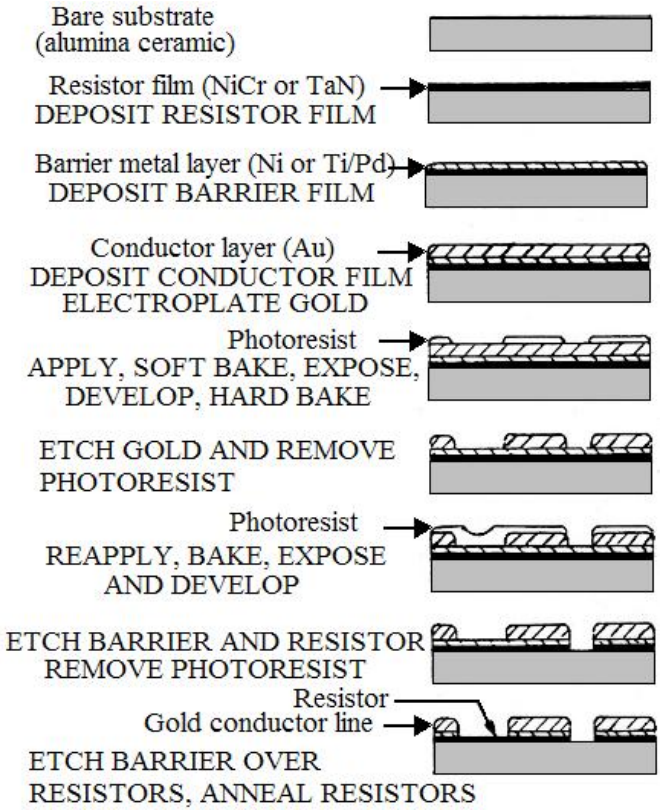

Fig. 3.2.43 Process steps

When the thin film substrate has been completely processed, resistors may be laser trimmed like in the case of thick film circuits. Thin film technology is very suitable for making precision R/C networks. Diodes and transistors can also be fabricated. After this, components will be mounted on the substrate. Integrated circuits are normally mounted in the form of naked chips that are glued on to the substrate and wire bonded. Discrete resistors and capacitors are normally mounted with conductive adhesives for electrical and mechanical contact and not soldered. In most cases, the complete circuit will be mounted in a hermetic package that is made of metal, or in some cases of ceramic. Terminal points on the substrate will be connected to the leads of the package by wire bonding. A welded or soldered metal lid on the package ensures hermeticity and good reliability.

An extension of conventional thin film technology is the multilayer thin film. It consists of many conductor layers that makes possible to achieve a very high circuit density. It may also achieve controlled characteristic impedance and good high frequency properties. The normal substrates are either 99.6% alumina or silicon wafers. Figure 3.2.44 shows a cross section. The dielectric most often used is polyimide or benzocyclobutene.

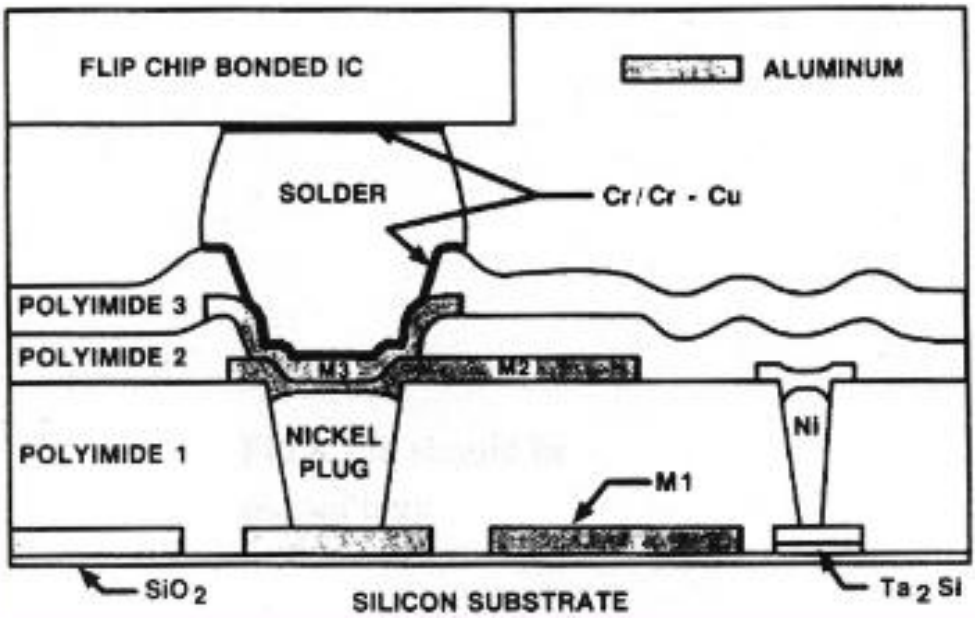

Fig. 3.2.44 AT&T structure for multilayer thin film

The organic dielectrics are deposited in a similar way as the photo resist to a thickness of approximately 10µm. Some of these materials are photo immagible, which means that they can be patterned without the use of an additional photo resist. The dielectric constant as well as the dielectric loss for these materials is low which means that good high frequency performance may be obtained. Also non organic materials like silicon oxide and silicon nitride are used for dielectrics. These materials are deposited by chemical vapour deposition or sputtering. These materials will typically be deposited in a thickness of the order of 1mm. The dielectric constant is significantly higher than for the organic materials. On the other hand, these dielectrics give a hermetically sealing of the metal tracks.