

2. Packaging materials

2.1 Introduction

As presented in the first chapter, the electronic packaging is defined as the engineering and manufacturing knowledge required to convert an electronic circuit/schematic diagram into a manufactured product of high quality and high reliability. The complexity degree of the electronic packages goes from integrated circuit package to printed circuit boards and, more, extends to electronic subsystems and systems. In a wider approach, any sensor or MEMS can be considered as an electronic package of level 1. The evolution in the field of integrated circuits is characterized by the increase of working frequencies, increase in component density, size reduction and increase in I/O pin count.

One major characteristic of the electronic packaging is the interdisciplinary character of the technical knowledge implied, which requires a multi-criteria approach. In this sense, the thorough knowledge of materials involved in electronic packaging is of maximum importance. As it is well known, in packaging various types of electronic materials are employed. A classification based on a unique criterion is difficult to be realized, but the materials are basically metals, ceramics and plastics.

- **Metals**

Metal provides the ultimate gas and moisture barrier that can convey lifetime values predicted to be more than 100 years.

Although raw metals can be quite inexpensive, the fabrication methods used for packages generally add substantial cost. So while metal is the gold standard, this is unfortunately reflected in the price. But, metal packaging, because it is typically electroplated, can release contaminants such as hydrogen; devices that are sensitive to hydrogen may use hydrogen getters within the metal enclosure. Metal and metal composites are presently used as the electrical conductors for devices, packages and PCB interconnects, but this could change in the future as nanotechnology and organic conductor advance. A process called injection molding metal (IMM) might offer some savings to metal packaging, but the electrical conductivity of enclosures, regardless of how they are made, requires insulation and special processes that add cost.

- **Ceramics**

Ceramic continues to be a popular material for hermetic and certain non-hermetic packages that need the following attributes: good planarity, smoothness, extreme mechanical stability, high thermal conductivity, and excellent temperature stability.

Ceramic materials and processes continue to be more expensive than organic technology although cost-reducing processes are still evolving. Ceramic is presently the favoured platform for large CPUs and the preferred cavity type enclosure for MEMS, MOEMS (Micro-Opto-Electro-Mechanical Systems) and some RF (radio frequency) devices. But ceramic is being replaced by plastic materials wherever possible for cost reduction and manufacturing simplicity.

- **Plastics**

Plastic packaging, primarily based on thermoset materials, accounts for perhaps 95% of the world packaging market because of low cost, versatility, and easier automation. But there are issues. The common EMCs have limited shelf life, must be kept in cold storage to extend useful life, and can produce variable properties depending on age and temperature history during

processing. EMC materials can have surprises as happened when material that appeared to be good, resulted in failures of a large number of products in 2000-2001 that triggered a host of expensive lawsuits and settlements. The complex mixture nature of EMCs and its multiple polymerization reactions can make quality control difficult.

Thermosets, once polymerized, cannot be melted for reuse and become scrap. Worse yet, EMC is generally classified as hazardous waste making disposal increasingly difficult. Many EMCs contain bromine flame retardant compounds that are destined to be regulated into extinction just like lead solders. Some bromine compounds fall under European RoHS rules and others will almost certainly be restricted in the future. Replacement of bromine with other choices like phosphorus as a flame retardant will only add more uncertainties. Reformulating will require retesting and a “reset” of the learning curve.

Epoxies are also relatively poor gas and moisture barrier materials although chip passivation has allowed most devices to work well enough to bring success to the plastic package. What are the plastic material alternatives?

Impending regulations and the need for better performance have thrust thermoplastics into the centre stage of consideration.

Thermoplastics can be cheaper, environmentally friendly, reusable, recyclable, and boast near-hermetic properties far superior to non-hermetic epoxies. One of the best thermoplastic packaging candidates only contains carbon (C), hydrogen (H) and oxygen (O), yet passes flammability specs and survives lead-free solder temperatures (over 260°C). Thermoplastic properties are controlled and confirmed by the resin manufacturers who complete the polymerization reactions and deliver 100% polymer. Conversely, thermosets will vary from run to run since the end user is the polymer manufacturer who affects the final properties by carrying out in situ polymerization. Thermoplastics are much simpler and have more predictable chemistry than epoxies. Epoxies start as mixtures and typically undergo dozens of competing reactions during polymerization to form a myriad of intermingled structures that can be difficult to quantify. The problem with their complexity was perhaps demonstrated by the 2000-2001 epoxy packaging failure epidemic where allegedly bad material was not discovered until complete systems had been assembled and failed in the field. But the increasing need for lower cost cavity packages may be the driver for developing the new class of packaging based on thermoplastics. MEMS, MOEMS, some RF and OE (opto-electronics) have created an escalating demand for lower cost free-space enclosures that might be best satisfied by modern thermoplastics. Thermoplastics are also finding increasing favour as circuit dielectric materials, but mostly in the flexible circuitry domain that is also the fastest growing PCB segment. One classification can be done after the packaging level hierarchy.

Zero level packaging materials:

- Semiconductors;
- Attachment materials;
- Substrate materials.

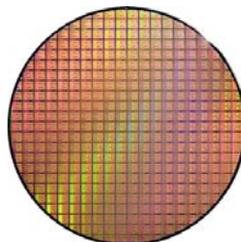


Fig. 2.1.1 Image of a wafer

First-level packaging materials:

- Wire for Bonds;
- Tapes;
- Case materials;
- Leads materials;
- Lid materials.

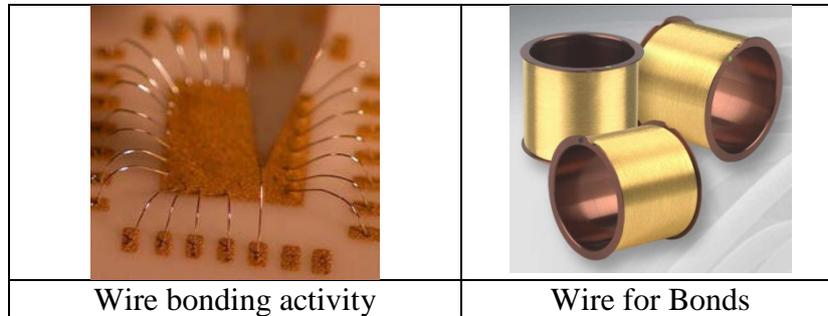


Fig. 2.1.2 Examples of first-level packaging materials

Second level packaging materials:

- Reinforcement fibre materials;
- Compounds and resins;
- Laminates;
- Flexible materials;
- Conformal coatings.



Fig. 2.1.3 Examples of second level packaging materials

Third level packaging materials:

- Backplane materials;
- Connector materials;
- Cable materials.



Fig. 2.1.4 Examples of cables

It is possible to make a classification of materials based on the application domain or on electrical properties, etc. We have in this sense:

Classification based on applications:

- Materials for Hybrid circuits;
- Materials for LTCC;
- Materials for SMD, Materials for PCB;
- Materials for PV cells, etc.

Classification based on electrical properties (conductivity):

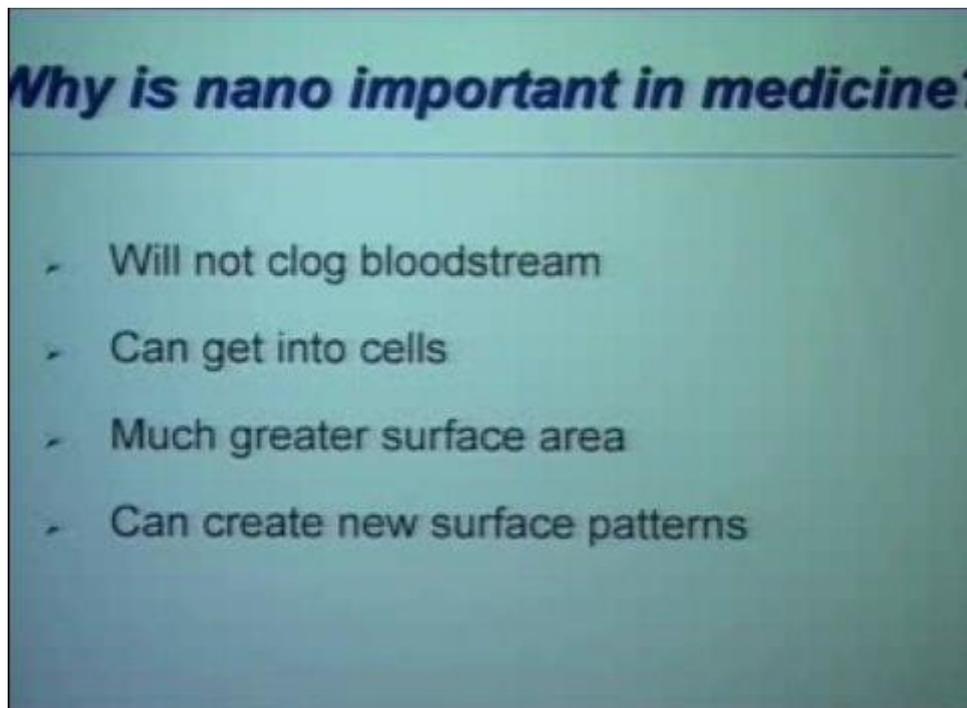
- Conductors;
- Semiconductors;
- Insulators (Dielectrics) – Polymers, Ceramic, Glass, Others.

2.1.1 Materials for Packaging Technology

Thermoset epoxies, discovered nearly 80 years ago, remain the workhorse material for most electronic packages. However, this may change with the ever-increasing technical and economic challenges along with the dramatic shift to “green materials” driven by RoHS and other environmental regulations. Modern halogen-free thermoplastics can now boast excellent thermomechanical properties and fabrication with highly automated high-efficiency high-volume processes. Plastic injection molding can readily produce precise and intricate 3D structures suitable for electronic, photonic and micromechanical packaging. Although there is a well-established packaging infrastructure tied to traditional thermoset epoxies, there is a much larger worldwide manufacturing base that excels in shaping thermoplastics. This is the ideal time to evaluate thermoplastic materials for packages and interconnects for the 21st century technology.

The signal and power distribution requires appropriate use of materials to form the system-level packaging hierarchy. Power distribution, for example, requires metals with the highest electrical conductivity for the least voltage drop. Heat transfer requires materials having the highest thermal conductivity. The minimized delta-I noise requires low inductance and high capacitance power distribution. High performance computers require high-speed signal propagation, which requires the use of the lowest dielectric constant, dielectrics in which to embed the best electrical conductors. Materials are also required to join ICs to form IC packages as well as to join materials to form precise electrical structures with the required impedance, capacitance, resistance and inductance.

Continued miniaturization, increased performance, as well as increased reliability of micro-systems require development of new materials and manufacturing methods (watch the presentation film from below, created by Invitrogen-UC San Diego Frontiers in Biotechnology, to understand the basics of the new materials called biomaterials).



Biomaterials and how they can change our lives
(<http://www.youtube.com/watch?v=OrodZiIWQeY>)

2.1.2 Non-woven fabrics from electrospun nanofibres

Electrospinning of plastic and ceramic nanofibers, through a rheological instability of charged polymer melt droplets in an intense electrostatic field, has been scaled to industrial production of nanofiber products. The nanofibers, featuring 10-100 nm diameters and macroscale lengths, are 2-3 orders of magnitude finer than traditional textile fibers and human hair, and can be made of a variety of nylon, polyesters, polyamides, acrylics etc. as well as biomolecules of proteins, collagen etc. Randomly laid aggregates of nanofibers in non-woven bundles, membranes and bulk structures exhibit high porosity, small interstitial size, high surface area resulting in high absorbency and reactivity to chemically functional groups.

Today, one of the major bottlenecks hampering continued development of micro-systems is effective dissipation of the heat generated by integrated circuits, MEMS devices, etc. It is essential that micro-systems can operate within their designated temperature interval. Operation at too high temperatures may cause deterioration of semiconductor performance as well as fracture, delamination, melting, creep, corrosion, electromigration and even burning of packaging materials, reducing the reliability and projected lifetime significantly. As integration density follows Moore's law, the amount of heat generated by microelectronic systems roughly increases exponentially. Consequently, there is a need for the industry to develop highly thermally conductive materials which facilitate effective heat dissipation, and implement these materials into manufacturing processes rapidly.

A well designed thermal management system will keep operating temperatures within acceptable limits to optimize device performance and reliability. With decreasing the thickness of the thermal interface material (TIM), thermal resistance decreases. Using proper material, the thermal resistance can even decrease dramatically. It has been shown that the interface resistance between the filler and the matrix could arise because of imperfect wetting and mixing of the particle with the polymer matrix. It is also readily demonstrated that the interface resistance is actually comprised of contact resistances plus the bulk resistance of the TIM. Clearly, thinner interfaces and higher conductivity improve the situation. Increasing chip power densities require thermal interface materials with lower thermal resistance. This situation motivates an exploratory research on development of nanoparticle based interface material at Electrovac. A thermal grease combining carbon nanotubes as fillers and resin as matrix do deliver an ideal thermal performance as described in previous work.

Carbon nanotubes (CNT) are superior thermal conductors by themselves. The longitudinal thermal conductivity, 3000W/mK for a multi-walled nanotube, has been measured at room temperature. An unusually high value, 6600W/mK for an isolated nanotube, has even been suggested. But, the thermal conductivity of the CNTs composite will be much lower than the value estimated from the intrinsic nanotube thermal conductivity and the volume fraction. The interfacial resistance for the heat flow between the nanotubes and the matrix leads to a low thermal conductivity of the CNTs composite. Testing the dispersion of carbon nanofibres in different matrices will make it possible to take full advantage of the high thermal conductivity. Both high thermal conductivity and thin fibre diameter make carbon nanofibre an excellent filler material.

2.1.3 New Packaging Materials

In the next five years, development of several new packaging materials is critical. Some examples include low stress underfill to support large die sizes, ultra fine pitch bump and more

than 10 K bumps/die. Pressurized underfill is one technique showing strong promise. Vacuum under fill solutions for smaller die are also under evaluation, and there is potential for extended use for larger dies. These solutions, however, do not do much to enhance current technology-capillary fill. No flow and wafer-level fill hold much promise for larger, high bump count devices, so some additional driving force is necessary for successful fill-vacuum and/or pressure.

Thermal stability is a key issue, especially in the automotive environment, and the current material set, and perhaps the fundamental epoxy chemistry, will not meet requirements for 180°C continuous operations. Exploration of high junction temperature, >150°C, mold compound and die attach materials is underway as a solution to the challenge. This issue extends to RF modules as power density in RF devices is expected to increase dramatically over the next five years while the size continues to shrink. Highly conductive mold compounds and encapsulates to support RF modules have potential to help maintain thermal conductivity despite these changes.

Package substrates will also require considerable development and improvement, especially in high speed electrical transmission applications. For example, silicon substrate can reduce the size of the transmission line and the line width using lithography technology, and a minimum size transmission line can reduce resistance leading to high speed applications. Some other techniques that may prove successful include coreless thin substrates (wire bond and flip chip) with reduced metal layers to support thin packages and stacked die packages. Substrates with selected solder pre-coating and thin NiAu plating areas are another alternative.

Large format substrates are still experiencing manufacturability, warpage and board attach issues, and these issues need to be addressed. A very critical requirement is development of low-cost fine pitch flip chip substrates to achieve cost parity with wire bonded packages. This could be achieved by increasing wiring density per layer and reducing layer count.

There is also an emergence of lead-free and RoHS-compliant packaging and use of lead-free solders and ‘green materials.’ To address thermal requirements, new and exotic lid and lid attach materials will be developed. Solder lid attach, high k lids, micro-channels in the Si or lids and other solutions must have low resistance and excellent reliability for adoption in future packages.

Electronics can be conveniently divided into devices (chip; die) and interconnect structures (package routing, printed circuit, etc.). Electronic chip devices, with over 400-million transistors, are now fabricated in nanoscale (1-billionth of a meter) dimensions. MEMS (Micro-Electro-Mechanical Systems) and Optical MEMS (called MOEMS; add “opto” to the acronym) technologies have added mechanical and optical features to chips while retaining electronic functionality. MEMS chips are now used in cars, planes, rockets, military vehicles, cell phones, robots, medical devices, and many consumer products.

MOEMS, used in digital projectors, the cinema, and HDTV, can claim the title of the world’s most complex machine. A single chip contains millions of mechanical parts that are instantly moved under electronic digital control. A modern digital projector or state-of-the-art digital home entertainment centre can utilize a chip with 1,300,000 micro-mirrors that point either forward (pixel on) or off-axis (pixel off) to generate the images seen on the screen. The integration of logic, light, RF, and mechanical action on a monolithic device, all mass-produced, opens up a new epoch for technology that requires novel packaging.

Device-level advancements are certainly inspiring and even mind boggling, but these incredible chips MUST have a suitable interface to the outside world. The component package is the primary interface that must handle electrons for traditional chips, but also light and matter for

newer classes. Although the package can be viewed as conductor mated to an insulator platform, the huge challenge for industry is selecting the right materials for an optimized design that uses the best processes to cost-effectively manufacture billions of parts. The package plays a key role in the continuing high technology revolution.

Materials useful for packaging electronic components usually exhibit certain properties. For example, the packaging material should provide dissipation of static electricity and shielding from static discharges and electric fields that may be generated, e.g. when the electronic component moves inside the package or when the packaging material is rubbed against other materials. The packaging material should also function as a barrier against moisture, vapour and oxygen to protect the electronic component from degradation while it is being stored. BGA (ball grid array) housing is a way of packaging electronic components. A commonly used format for electronic packages is known as the “quad flat pack” where the leads which are provided to connect a semiconductor device to the remainder of the system are provided on four sides of the semiconductor device and are formed to a gull-wing shape. A typical electronic device package assembly comprises a relatively flat lead frame having a plurality of leads terminating at an interior opening. The electronic device to be housed is positioned in alignment with the interior opening of the lead frame and is electrically attached to the interior terminal ends of the leads by connecting wires. The device for packaging electronic components in BGA housings has a mounting frame, which frames and retains a plastic intermediate substrate. The plastic intermediate substrate has a plurality of contact bumps with connected conductor tracks that lead to a plurality of semiconductor positions inside the associated mounting frame. Miniaturization of packaging is of continuing interest as electronic components become smaller and smaller. It is also a goal in the field of packaging designs to provide modularization so that various sized enclosures can be generated using a minimum number of compatible mechanical components.

2.2 Plastic materials and processes

Polymers are long-chain molecules that occur naturally, but are now mostly synthesized. Plastics are, arguably, the most important materials of today. Materials have been so important to civilization that entire eras have been named for them; the Stone Age, Bronze Age, etc. From a materials perspective, we are still in the Plastics Age and the day will come when we have plastic (organic) electronic devices in polymer enclosures on plastic circuits in plastic housings. Ironically, many who worked with polymers 20 or 30 years ago were told, and many believed, that the golden age of polymers had passed *because all the basic polymers had been invented*. How wrong! Fundamentally new polymers continue to be invented, innovative processes are still being implemented and imaginative new products come to the market every month. Much of the emerging nanoelectronics is based on organic, polymer-like structures that may someday replace wires and silicon transistors.

Although electronics has been considered the leading edge of technology, this field is far behind in the adoption of modern polymers except for the housing, cases and enclosures that hold the electronics products.

2.2.1 Thermosets vs. Thermoplastics

Thermoset plastics, like epoxies, are produced when monomers react to form long chains that are interlinked (cross-linked) to create mega-molecules. Epoxies were the first broadly successful organic packaging materials and continue as the most widely used materials today.

They are also used to make organic circuit laminates like FR-4 and BT. Since epoxies are thermosets, they are “set” by polymerization when heated to about 150°C or higher (ambient cure is also possible but properties will be different). The other major polymer class is thermoplastics, polymers that can be melted and remelted by heating since there are no confining cross-links. The key distinction between thermosets and thermoplastics is the cross-link.

A cured epoxy part is more or less one giant molecule that can't melt. It was the non-melting characteristic that made them a good choice for packages and circuit boards that needed to withstand the high temperatures of soldering. Early thermoplastics would soften and deform at soldering temperatures, but there is no problem for today's advanced materials.

Many now feel that the thermoset class of polymers, especially epoxies, has reached a plateau and will continue to fall short as packaging and PCB requirements increase. Relatively high moisture absorption is an increasing concern and so is the need to add flame retardants. But epoxies are still the dominant polymers for electronics and are used in plastic packages, encapsulants, underfills and circuit boards. While epoxies are notable for their balance of properties, they don't really excel in any particular area. In fact, without a significant level of fillers and modifiers, epoxies can't be used in electronics.

Substantial amounts of organic bromine compounds have been added to pass flammability standards. Encapsulants and underfills typically contain more filler than epoxy resin to tame the high CTE (Coefficient of Thermal Expansion) that ranges around 80 – 90 ppm/°C. And when it comes to water absorption, they are a “sponge” compared to many other commercial polymers. Epoxy-based circuitry laminates require a substantial level of glass reinforcement to control their dimensional instability as well as bromine for flame retardancy.

2.2.2 Transfer molding thermosets

The transfer molding process has been used for about 50 years to encapsulate electronics and is the *de facto* standard. The steps are straightforward: a chip is attached to a lead frame that is normally a strip or an array of chip bonding sites. Polymer adhesive is the usual die attach material and it can be dispensed at the wire bond station. Once the adhesive is quickly hardened by heating, wire bonds are made between the chip pads and the corresponding lead frame bond sites. The “loaded” array (or strip) is now placed into the molding tool. The transfer mold consists of a heated chamber that is separated from the cavities but connected to each one through a system of runners and gates. The process begins by closing the loaded mold. Thermoset epoxy molding compounds (EMC), in the form of solid pre-heated preform (called a puck), is moved into the chamber and heated to melting. An auxiliary ram then pushes the liquefied material through the runner and gates into the cavities, completing the transfer process and encapsulating the chip and lead frame. Post heating may be required to fully-polymerize the epoxy.

2.2.3 Thermo-shaping of thermoplastics

Thermoplastics also have long chains but they are independent (not cross-linked) so that thermal energy will cause a transition from solid to liquid state, while cooling returns the material to the original solid state with virtually no intrinsic property changes. Thermoplastics can therefore be reshaped because of this reversible phase change and this is the basis for injection molding and other thermoforming processes. Plastic thermoforming is a very large

world-wide industry that is highly diversified. Today's thermoplastics are superior to EMCs in critical categories and can take the abuse of lead-free soldering, can have an order of magnitude better moisture resistance, are rapidly shaped into precise 3D structures, and many pass flammability standards without adding halogens, phosphorus, nitrogen compounds, or hydrates.

2.2.4 Injection Molding

The Injection Molding (IM) press first softens the plastic resin, injects it into a metal mold that can have 100 or more package-shaped cavities, and then finally ejects finished parts. The cycle is repeated. A complete IM cycle for a package array takes about 10 seconds. The hot molten plastic is quickly cooled by the mold to form a tough solid part that will not melt during soldering. IM, one of the most ubiquitous manufacturing processes, is used around the world to produce very large and near-microscopic parts for every industry, including automotive and electronics. One drawback is that large, multi-cavity molds can be expensive. Plastic injection molding is well-suited for electronics and several companies now offer molded cavity style packages made from high-temperature plastics such as LCP (Liquid Crystal Polymer) or PPS (Polyphenylene Sulfide). The thermoplastic shaping processes have also kept pace. Injection molding can produce tens of thousands of packages in an hour – all automatically. Micro-molding has advanced to a level where precision parts can only be identified under a microscope. One of the most valuable features of IM is that it can readily produce complex 3D cavity style package structures. Injection molding can form a strip or array of cavity BGA packages at high-volume and low cost using economical engineering plastics like LCP. This polymer class is not new but has been recently popularized as a new flexible circuitry substrate. Any waste, such as mold runners, can be remelted and reused.

Although thermoplastics can be used for overmolding and contact encapsulation, this is probably not a good option for this class of materials. Since thermoplastics must be heated to their melting points that must be high enough to withstand solder reflow, the chip and interconnect would be exposed to very hot and often viscous melt. Only a few discrete devices are overmolded with thermoplastics today. The best fit for thermoplastics is pre-molded packages. Although post-molded packaging is the norm, pre-molded designs can have good economics while offering much greater versatility.

2.2.5 Wire bonding materials

Wire bonding materials used in a ball bonding process mainly include the bonding wire and bonding tool. Ball bonding tools are called capillaries, which are axial-symmetric ceramic tools with vertical feed holes. Figure 1 shows an example of a capillary used in applications. The tool's tip is shaped to give the clearance needed in fine-pitch bonding.

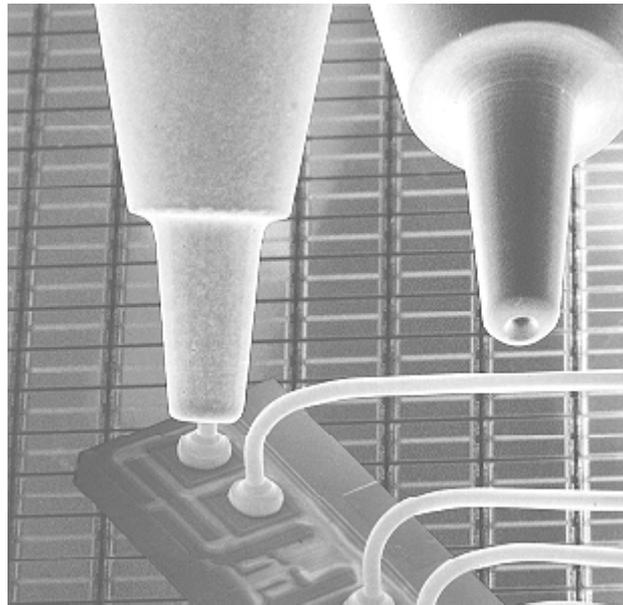


Fig. 2.2.1 Wire bonding tools

Figure 2.2.2 outlines the critical dimensions of a capillary, which include the tip diameter (T), angle of the bottom face (FA), outside radius (OR), hole diameter (H), and chamfer diameter (CD). The tip usually is determined by an application's pitch. FA and OR affect mainly second bond, while the hole and chamfer diameters affect both the first and tail bond formations. These are the most critical dimensions of a capillary.

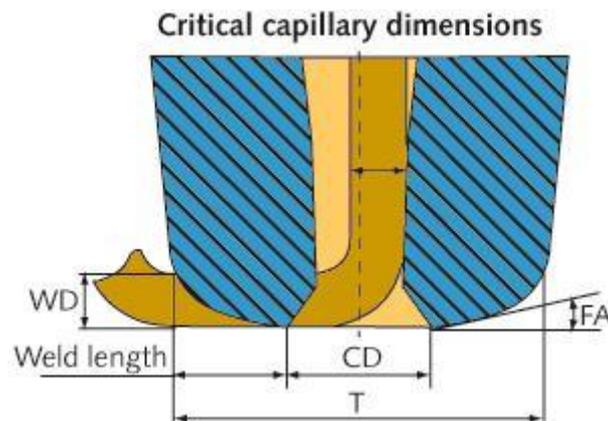


Fig. 2.2.2 Critical capillary dimensions

Most bonding wire used in ball bonding is gold (Au) wire of 99.99% purity, which is often referred to as 4Ns wire. Alloy wires (99.99% or less purity) are sometimes used to meet special application requirements, such as high wire strength. Studies have shown that certain dopant (impurity in the wire) can slow Au-Al intermetallic growth. 3Ns and 2Ns wires are sometimes considered to improve device reliability.

A special consideration for bonding wire is its heat-affected zone length, which is related to the recrystallization process due to the heat. The heat-affected zone often weakens the wire. A longer heat-affected zone in the wire often results in higher loop height. Some applications require high strength and a low heat-affected zone, as shown in Figure 2.2.3.

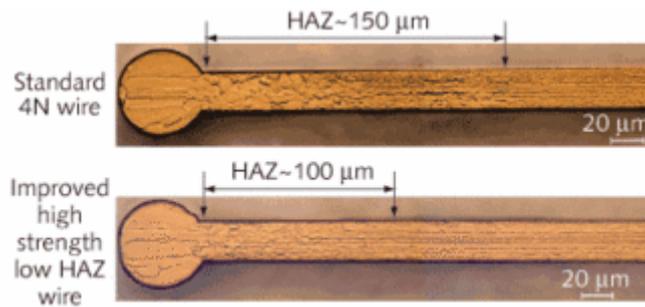


Fig. 2.2.3 Certain high-strength wire offers shorter heat-affected zone (HAZ) and improved looping capability

Copper (Cu) wires can be bonded with some modifications to the wire bonder. The modifications mainly consist of using a forming gas environment to prevent Cu oxidation during the free air ball formation. Both Au and Cu bonding are done at an elevated temperature (normally 150° to 240°C, depending on the device). This process is called thermosonic bonding because of the use of heat and ultrasonic energy.

2.3 Dielectric materials used in the manufacture of printed circuit boards

In a level 2 Electronic Packaging, a lot of dielectric materials are available for use. Of maximum importance is the dielectric for a particular printed circuit board. The task has always been clouded by a confusing array of materials choices, equally confusing claims by the manufacturers of those materials, confusion about what the actual requirements of an application are and a substantial collection of misinformation circulating in the design and fabrication communities. The goal of material selection should be to choose a material that adequately handles the signalling task and, at the same time, achieves the lowest overall PCB cost.

This task has been further complicated in recent years by the increasing clock frequencies of PCs and by the drive for gigabit and beyond data rates in Ethernet related products. Questions arise almost daily about whether FR-4 based materials can serve in these applications.

2.3.1 Two major applications areas, RF/analog and digital

Electronic packaging can be divided into two major applications areas, each of which has its unique requirements. The requirements are sufficiently different that two classes of materials have been developed to meet their needs. Understanding these areas and their requirements are basic to making the correct material choice.

The two major applications areas are RF/analog and digital. The major differences between these two areas are the ability of the circuitry involved to tolerate signal losses and the complexity of the circuitry (see the presentation film from below, created by Georgia Tech - Microelectronics Research Center, as an example of technology in the RF domain).



Plasmatherm RIE device (<http://www.youtube.com/watch?v=mWz42gMOI7w>)

a. RF/Analog circuit characteristics

RF/analog circuits are usually processing signals that are small or precise. The accuracy with which the circuits perform or the ability of the circuits to process low level signals successfully depends on a package with the lowest possible losses. Losses occur as reflections where impedances change and from absorption of some of the signal in the dielectric materials. The latter can be a significant consideration when choosing a dielectric for this type of product.

Losses from reflections are traceable to variations in impedance. These stem from variations in laminate thickness, variations in dielectric constant of the laminate and variations in final etched trace width. The first two are traceable to characteristics of the laminate itself. The latter is traceable to process uniformity at the manufacturer.

The complexity of RF/analog circuits is low enough that PCBs with two or three layers can be used to house most them. Thus, the ability of a material to laminate in many layers is less important than are losses, dielectric constant and dielectric constant uniformity.

b. Digital circuit characteristics

Digital circuits are designed to tolerate substantial signal loss and still perform their tasks successfully. As a result, material characteristics other than losses tend to be more important. Digital circuits are usually quite complex and require several or many signal and power layers to house them. This puts a priority on processing characteristics such as ease of lamination, ease of drilling and other processing steps. The need for many layers in some designs causes the PCB to be relatively thick. Soldering and reworking these thick PCBs puts significant thermal stress on the vias and other plated through holes. In order to insure the PCB will not fail because of this, the temperature characteristic, T_g , must be high enough to withstand these processes.

Riding on top of the above needs, digital PCBs tend to be used in products that are subjected to intense price pressures. As a result, costs of the raw laminate and processing costs place an additional demand on the choice of laminate materials used.

2.3.2 Two Major Materials Classes

PCB dielectric materials can be divided into two major classes based on the type of reinforcement used. These are woven glass reinforcements and non-woven glass reinforcements. Woven glass reinforced laminates are lower in cost than non-woven laminates and are cheaper to produce and process. Because of the amount of glass in the woven glass cloth, the dielectric constants of laminates based on it are higher than laminates based on other reinforcements. (The glass used in laminates has a relative dielectric constant of 6.0.)

A number of laminate properties can be important depending on the application. Most materials have been developed to optimize one or more of these properties. Among these are:

Relative Dielectric Constant, ϵ_r - this property is a measure of the effect an insulating material has on the capacitance of a conductor embedded in or surrounded by it. It is also a measure of the degree to which an electromagnetic wave is slowed down as it travels through the insulating material. The higher the relative dielectric constant, the slower a signal travels on a wire, the lower the impedance of a given trace geometry and the larger the stray capacitance along a transmission line. Given a choice, lower dielectric constant is nearly always better.

The dielectric constant of nearly all PCB dielectrics changes with frequency and usually goes down as frequency goes up. This manifests itself in two ways in transmission lines. The velocity of signals increases as the frequency goes up, resulting in phase distortion in broadband amplifiers. Broadband RF and microwave amplifiers usually need to be made from laminates with relative dielectric constants as flat with frequency as possible to minimize this problem.

The impedance of a transmission line goes down as frequency goes up resulting in faster edges reflecting more than slower ones. The main effect this has is to cause errors in impedance calculations and measurements. As an example, if the relative dielectric constant measured at 1MHz is used to calculate impedance and a time-domain reflectometer (TDR) with a 125 picoseconds rise time is used to measure the impedance, there will be disagreement due to the fact that two very different frequencies have been used. Figure 2.3.1 illustrates how relative dielectric constant varies with frequency for some typical PCB laminates.

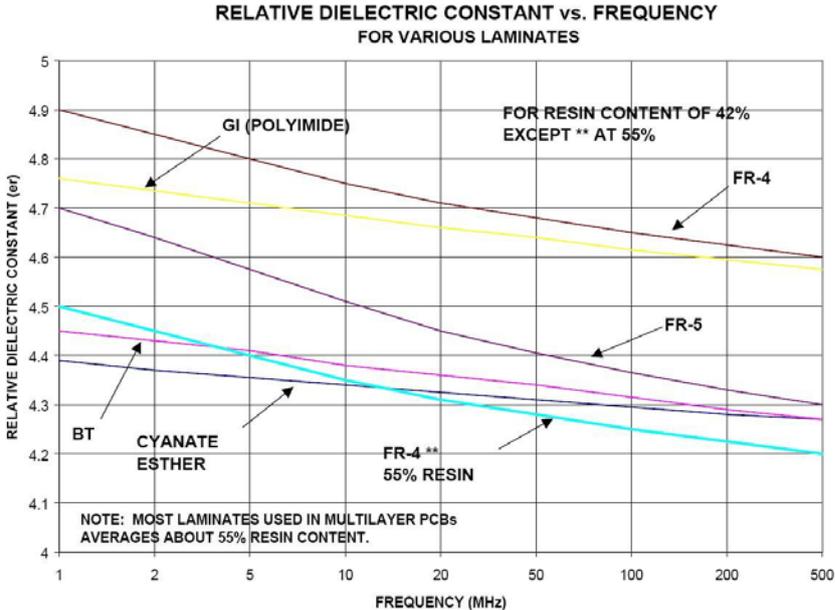


Fig. 2.3.1 Relative Dielectric Constant vs. Frequency for Several Laminate Types

Another source of relative dielectric constant variation is the ratio of reinforcement or glass to resin used to make a laminate. Figure 2.3.2 shows how the relative dielectric constant of a standard FR-4 laminate changes with the ratio of glass to resin. This chart is based on measuring relative dielectric constant at 1MHz. Many of the disconnects between predicted impedance and measured impedance stem from that fact that the relative dielectric constant for one glass to resin ratio is used to calculate impedance and the actual glass to resin ratio of the material used to fabricate the PCB is different. As an example, the relative dielectric constant 4.7 is for FR-4 with 42% resin measured at 1MHz. Most multilayer materials contain about 55% resin. Typically, impedance of the finished PCB is measured with a TDR of edge rate about 150 picoseconds which corresponds to about 2GHz. The relative dielectric constant for this pair of conditions is approximately 4.1. These two sets of conditions, when used on the same PCB, one to calculate the other to measure, can result in an impedance error of as much as 5 ohms in a 50-ohm system.

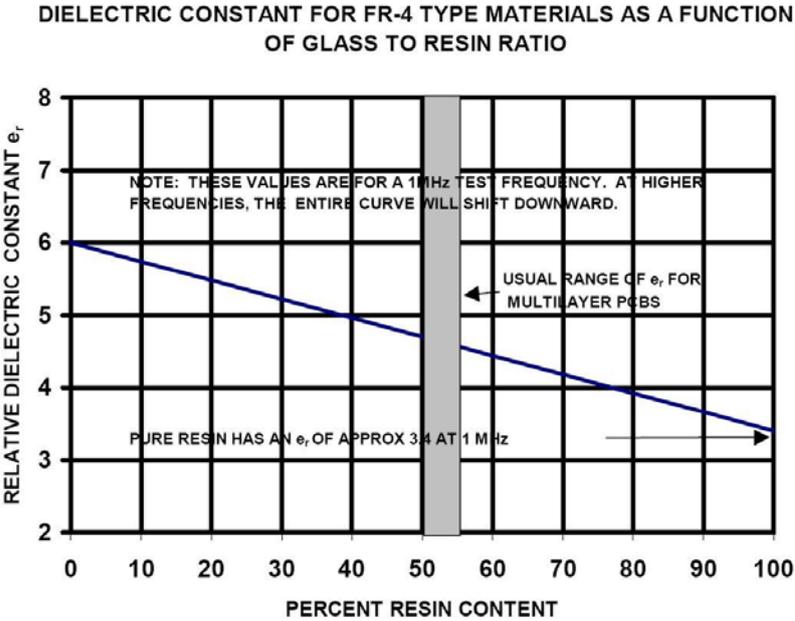


Fig. 2.3.2 Relative Dielectric Constant vs. Glass to Resin Ratio for FR-4

Glass Transition Temperature, T_g - all common laminate resins exhibit changing temperature coefficients of expansion as temperature increases. Figure 2.3.3 shows this characteristic for a number of common multilayer laminates. Glass transition temperature or T_g is the temperature at which the temperature coefficient of expansion makes a significant change from a low value to a much higher value. This corresponds to a phase change in the resin system.

Notice that the temperature coefficient of expansion at low temperatures is close to that of copper and glass, the two reinforcements in the X and Y directions of a PCB. When the temperature of the composite material system in a PCB exceeds its T_g, the resin part of the package begins to expand at a much more rapid rate than either the copper or the glass. Since the resin cannot expand in either the X or Y directions, virtually all the volume growth takes place in the Z-axis. The vias and other plated through holes are oriented in the Z-axis and are placed under stress as soldering takes place. The combination of thicker PCBs and multiple soldering operations can produce failed PCBs even before they complete the manufacturing process. Care must be exercised in choosing the proper T_g material for each application.

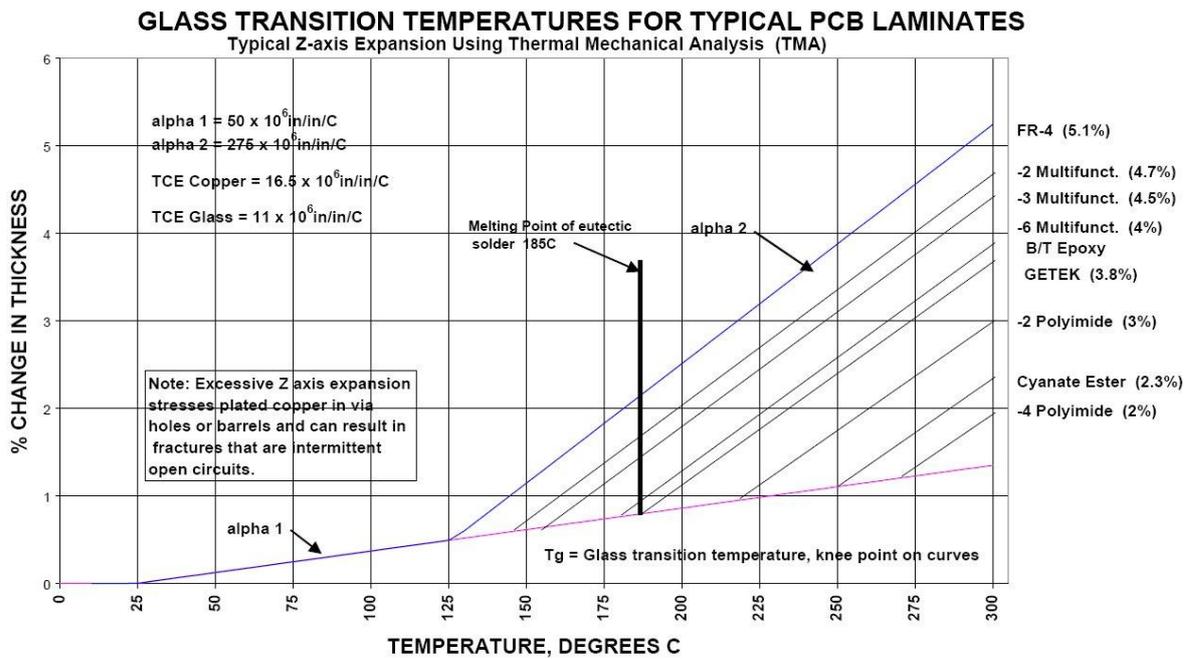
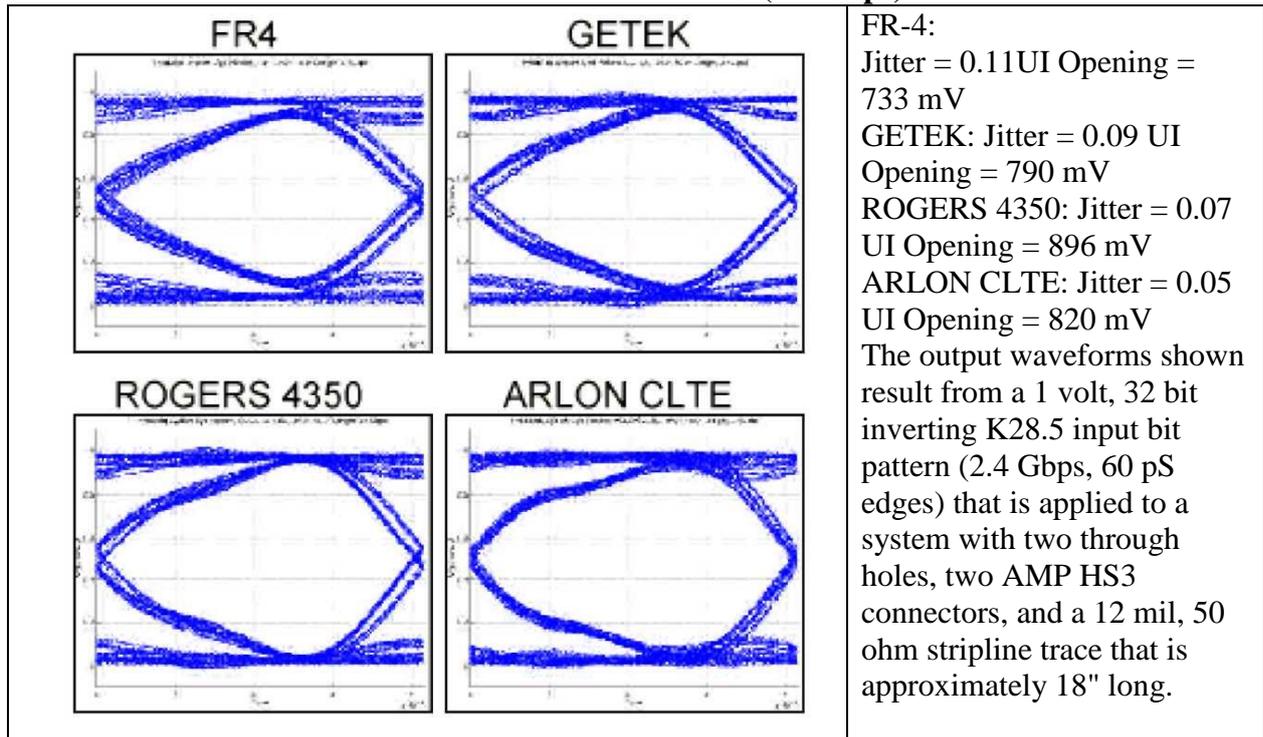


Fig. 2.3.3 Glass Transition Temperature Curves for Various PCB Laminates

Loss tangent - Loss tangent is a measure of how much of the electromagnetic field travelling through a dielectric is absorbed or lost in the dielectric. This property is one of the least well understood of all those that characterize laminates. As a result, ultra low loss materials are often used in digital applications when they are not needed. This results in increased PCB cost without a corresponding benefit.

Figure 2.3.4 shows the classic “eye diagram” used to measure the performance of an Ethernet link. It was created by Amp Packaging Systems as a measure of the performance of four potential laminate materials. The test environment is a 2.4 Gigabit per second backplane with 18" long paths. The materials examined are high temperature FR-4, GETEK from GE, RO 4350 from Rogers and CLTE from Arlon. These materials have loss tangents of .02, .015, .008 and .004 respectively. From this diagram one can gage the improvement in signal size as lower loss materials are used. Even at 2.4 Gigabits per second, the FR-4 material delivers a satisfactory logic signal. This may come as a pleasant surprise to those wishing to use FR-4 based materials for gigabit and higher products and as an unpleasant surprise to those who thought that a lower loss, more expensive material was needed.

SYSTEM EYE PATTERNS (2.4 Gbps)



Courtesy AMP Circuits and Design

Fig. 2.3.4 Ethernet Eye Diagrams showing losses in 18" long 2.4 Gigabit links using four types of dielectric materials

Dielectric Breakdown Voltage, DBV - Dielectric breakdown voltage is a measure of an insulator's ability to withstand the stress of high voltages placed across it. From Table 2.3.1, it can be seen that all of the commonly available laminates have at least 1000 volts per mil of thickness DBV. This means that a 2-mil thick laminate can withstand a voltage stress as high as 2000 volts, more than adequate to meet the Telco specifications applied to many networking products.

Moisture Absorption - All resin systems absorb some moisture or water when exposed to high humidity environments. This absorption affects the PCB in two ways. Water has a relative dielectric constant of approximately 73. If a laminate absorbs a significant amount of water the resulting relative dielectric constant of the combination will be higher than the 4.1 used to calculate impedance and can cause impedance mismatches.

A more important effect of moisture absorption is increased leakage current. Materials with high moisture absorption may exhibit leakages in excess of what the circuits housed on them can withstand. In order to use high absorption materials in such applications, it is often necessary to seal them with a special coating after first baking them dry. This represents an added cost as well as a problem when rework must be done, since the coating must be removed to do the rework and then reapplied. Two materials that have this problem are polyamide and cyanate ester.

The moisture absorption levels of the FR-4 derivatives are satisfactory for all digital applications.

2.3.3 Goal of each application area

As noted earlier the two applications areas, RF/analog and digital have somewhat different materials requirements.

RF/Analog applications are characterized by the need for low dielectric losses, low leakage, a need for a low and uniform dielectric constant accompanied by a low layer count. Further, since this type of PCB tends to be small, cost of the dielectric material has less effect on overall product cost than do other cost components. As a result, using more expensive materials to meet performance goals is acceptable. For this class of PCBs, choosing a material based on its dielectric constant characteristics and losses usually dominates over other considerations.

Digital applications are characterized by high layer counts and large numbers of drilled and plated holes. The processing costs associated with registering and laminating many layers, coupled with drilling and plating ease usually dominate the choice of materials. Absolute dielectric constant value of the insulating material is important, but less important than processing costs and dimensional stability. As a result, woven glass reinforced materials are nearly always required. The choice of resin system used with the glass reinforcement is made based on keeping Z-axis expansion within acceptable limits. The thicker the PCB, the higher the T_g must be to produce a reliable PCB. Digital applications are nearly always subjected to pricing pressures, so material choices must be made in order to achieve performance requirements without adding extra cost.

An exception to the above rule for digital PCBs occurs when layer counts become extremely high as often occurs with supercomputer products. In order to keep the overall PCB thickness within reasonable limits and still achieve impedances in the 50 ohm range, it is necessary to use laminates without glass. Omitting the glass results in lower dielectric constants and higher impedance with thinner laminates. Dimensional stability is achieved by mating signal layers with power planes on opposite sides of a piece of laminate. The sheet of copper provides the dimensional stability during processing and lamination. Cost of the finished PCB will be higher using this strategy.

One other area that can require the choice of a low dielectric constant material is in ultra-fast switching applications such as gigabit and higher clocked systems. In such products flight time along the wires required to connect components may limit how fast the system can operate. As dielectric constant decreases, the speed of signal travel on a PCB trace increases. A material with a dielectric constant lower than FR-4 or other glass reinforced materials, such as Speedboard may be needed. It should be noted that this increase in speed carries with it a much higher cost PCB. A designer is advised to try all other methods for achieving the desired speed before resorting to this solution.

2.3.4 List of woven glass materials used in digital applications

Table 2.3.1 is a list of several commonly available glass reinforced laminates used to fabricate multilayer PCBs. It is arranged in order of increasing T_g or glass transition temperature. Glass reinforced Teflon is listed at the bottom for comparison purposes. Teflon is rarely used in multilayer applications due to the difficulty of laminating with it. The characteristics listed are for a resin content of 55% and with dielectric constant obtained using a TDR to measure the

velocity of travel rather than the parallel plate method at 1MHz. Notice that the dielectric constant ranges between 3.9 and 4.1 for all of these materials systems.

Material	T _g	ε _r *	Tan (f)	DBV (V/mil)	WA, %
Standard FR-4 Epoxy Glass	125°C	4.1	0.02	1100	0.14
Multifunctional FR-4	145°C	4.1	0.022	1050	0.13
Tetra Functional FR-4	150°C	4.1	0.022	1050	0.13
Nelco N4000-6	170°C	4	0.012	1300	0.10
GETEK	180°C	3.9	0.008	1100	0.12
BT Epoxy Glass	185°C	4.1	0.023	1350	0.20
Cyanate Ester	245°C	3.8	0.005	800	0.70
Polyimide Glass	285°C	4.1	0.015	1200	0.43
Teflon	NA	2.2	0.0002	450	0.01
		* Measured with a TDR using velocity method. Resin content 55%			

T_g = glass transition temperature DBV = dielectric breakdown voltage

ε_r = relative dielectric constant WA = water absorption

Tan (f) = loss tangent

All materials with woven glass reinforcement except teflon.

Tab. 2.3.1 Several commonly available woven glass reinforced laminates

As it can be seen from Table 2.3.1, the major difference between materials is glass transition temperature, T_g. In fact, all of these materials, except Teflon, were developed in an effort to arrive at a material that is easy to process and low in cost while raising the T_g. The T_g goal is to get as close to the melting point of solder, 185°C, as possible. It can be seen that GETEK, BT Epoxy Glass, Cyanate Ester and Polyamide Glass all achieve the desired T_g. Unfortunately, all of these have processing problems that make them more expensive, sometimes much more expensive to use than the Epoxy based materials.

The original low cost PCB material was FR-4 with a T_g around 125°C. This temperature was too low to provide reliable plated vias in PCBs thicker than .062". Multifunctional FR-4, Tetrafunctional FR-4 and the "high T_g" FR-4, such as Nelco N4000-6, have been developed in an effort to preserve the ease of processing that these epoxy resin systems provide while raising the T_g.

The "high T_g" F-4 systems achieve T_g values in the 170°-180°C range, high enough to build reliable thick PCBs, thick being more than .062". It should be possible to fabricate reliable PCBs as thick as .250" using these materials. The goal of a reliable, thick PCB at the lowest possible cost is the result.

2.3.5 Nonwoven or very low glass content materials

Table 2.3.2 lists several materials designed to provide good performance in RF and microwave applications. As it can be seen, the dielectric constants cover a very wide range.

Selecting a material from this list for use in an RF/analog application is a far more complex task than choosing a material for a digital application. For example, the Speedboard products are aimed at being included with other multi-layer materials as part of a high performance design where lower is needed. The various Rogers products are aimed at satisfying a broad range of differing RF needs.

In all cases, these materials are more expensive as raw materials and more expensive to

process than the epoxy resin based glass reinforced materials. The potential gains, mainly in lower dielectric constant that would result from using these materials in a digital PCB are rarely, if ever, worth the added cost.

Material	T _g	e _r *	Tan (f)	DBV (Vmil)	WA %
Speedboard N	140°C	3	0.02	N/A	N/A
Speedboard C	220°C	2.7	0.004	N/A	N/A
Rogers Utralam C	280°C	2.5	0.0019	N/A	N/A
Rogers 5000	280°C	2.3	0.001	N/A	NA
Rogers 6002	350°C	3	0.0012	N/A	NA
Rogers 6006	325°C	6 to 10	0.002	N/A	N/A
Rogers RO3003	350°C	3	0.0013	N/A	N/A
Rogers RO3006	325°C	6 to 10	0.003	N/A	N/A
Teflon		2.2	0.0002	450	0.01
Information from manufacturer's data sheets.					

T_g = glass transition temperature DBV = dielectric breakdown voltage
e_r = relative dielectric constant WA = water absorption

Tab. 2.3.2 List of non-woven or very low glass content laminate materials

2.3.6 Conclusions

A wide variety of materials have been developed for use in the manufacture of PCBs. Each has its target applications. When used in these targeted applications, the resulting PCB will have the lowest cost possible while satisfying the performance and cost goals of application. Due to confusion about the needs of these applications, especially digital applications, higher cost, more difficult to process materials are often selected. The result is a product that costs more than it should without a compensating benefit.

In the digital space, the “high T_g” FR-4 laminates have a T_g sufficiently high that all the most demanding applications can be handled with them. There is rarely a need to handicap a design with one of the other more exotic materials systems.

2.4 Materials for lead-free products

The electronic industry is moving toward green manufacturing as a global trend. In the area of soldering, mainly driven by European RoHS (Reduction of Hazardous Substances), lead was banned effective July 1, 2006, except in some exempt items. This European legislation is followed by China RoHS which has similar list of banned materials, and its phase 1 implementation was effective March 1, 2007. In Japan, the legislative activities dealt with the reclamation and recycling of electronics. The Home Electronics recycling law came into force in April 1, 2001, and applied only to TVs, refrigerators and similar items. Although not specifically aiming at lead, this legislation effectively drove Japanese industry toward lead-free soldering process. Those legislation activities lead the trend and effectively drive the rest of the world toward lead-free soldering.

Due to the global trend of green manufacturing, lead-free becomes the main stream soldering choice of electronic industry. SnAgCu alloys are the prevailing choices, with SnCu (+ Y), SnAg (+ Y), and BiSn (+ Y) families also being adopted, where Y represents minor additive elements. The soldering processing window is narrower than that of Sn63, mainly due to the

elevated melting temperature of SnAgCu solder and the limited high temperature tolerance of components and boards. The high surface tension of Sn aggravates the difficulty in wetting, while the high reactivity of Sn puts more constraint in contact time allowed between molten solder and base metal or solder container. The creep rate of SnAgCu is slower at low stress, but faster at high stress than Sn63. This results in a longer temperature cycling life at low joint strain applications, but a shorter cycling life at high joint strain applications. Higher Cu content stabilizes the intermetallic compound (IMC) structure at interface between SnAgCu solder and NiAu. The high rigidity of SnAgCu solders enhances the fragility of joints, although significant improvement has been accomplished via low Ag or high Cu content or doping approaches.

Among the numerous lead-free solder options available, the following families are of particular interest and are the prevailing choices of industry: eutectic SnAg, eutectic SnCu, eutectic SnAgCu, eutectic SnZn, eutectic BiSn, and their modifications, as shown in Figure 2.4.1. Also shown in Figure 2.4.1 are the related applications including reflow soldering, wave soldering, and hand soldering. Their characteristics and potential performance in electronic applications are presented below.

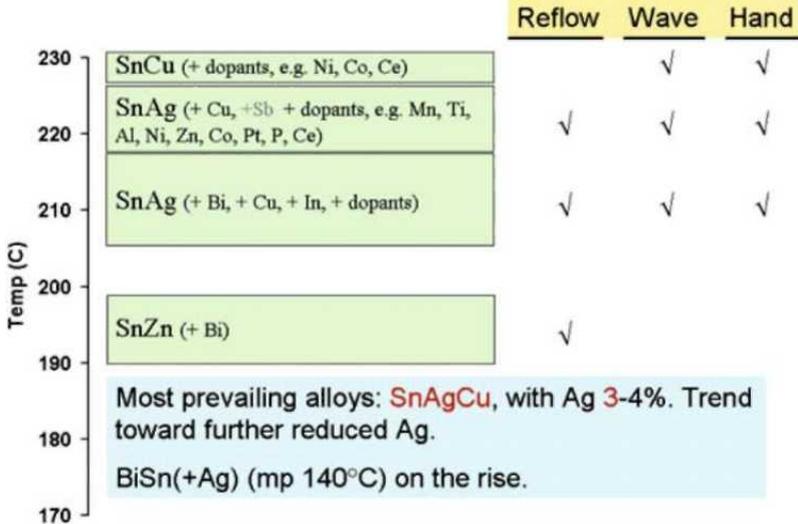


Fig. 2.4.1 Lead-free solder alloys and their applications

a. **SnCu (+ dopants, e.g. Ni, Co, Ce)**

Eutectic Sn99.3Cu0.7 exhibits a melting temperature at 227°C. Sn99.3Cu0.7 is lower in tensile strength but higher in elongation than both eutectic SnAg and SnPb, reflecting the softness and ductility of SnCu. The creep strength of eutectic SnCu is higher than Sn100, but lower than eutectic SnAg and SnAgCu at both 20°C and 100°C. Wetting balance test results by Hunt et al. indicated that the wetting ability decreased in the following order: eutectic SnPb > SnAgCu > SnAg > SnCu when an inactivated flux was used. Eutectic SnCu is commonly used at wave soldering and hand soldering.

The mechanical and wetting properties of eutectic SnCu were enhanced by adding a small amount of dopants such as Ni, Ge, Co, and Ce. Sn99.3Cu0.7-Ni0.05 + Ge (SN100C) and Sn99.5Cu0.5Co <0.05 (Cobalt995) were reported to exhibit a reduced wetting time, copper dissolution rate, and a shinier smooth solder joint surface at wave soldering. Sn99.3Cu0.7Ce0.02 was reported to have enhanced elongation performance and drop test performance.

b. **SnAg (+ Cu, +Sb, + dopants, e.g. Mn, Ti, Al, Ni, Zn, Co, Pt, P, Ce)**

SnAgCu (SAC) is the most prevailing alloy family for electronic soldering. Sn96.5Ag3Cu0.5 (SAC305), Sn95.6Ag3.5Cu0.9 (SAC359), ternary eutectic SnAgCu, Sn95.5Ag3.8Cu0.7 (SAC387), Sn95.5Ag3.9Cu0.6 (SAC396), and Sn95.5Ag4.0Cu0.5 (SAC405)

are all commonly used for reflow, wave, and hand soldering, and all exhibit a melting temperature around 217°C. Among those, SAC305 is the most popular one in Asia, and is also endorsed by IPC. Eutectic Sn96.5Ag3.5 is commonly used as well with a melting temperature 221°C.

For SnAgCu, its hardness, tensile strength, yield strength, shear strength, impact strength, and creep resistance are all higher than eutectic SnPb (Sn63). The wetting performance is better than both eutectic SnCu and eutectic SnAg, although poorer than that of Sn63. Addition of Sb into SAC, Sn96.2Ag2.5Cu0.8Sb0.5 (CASTIN), was reported to exhibit a slower intermetallic compound growth rate.

Due to its high hardness, lead-free solder joints typically suffer fragility issue upon drop test. This is a particular concern for portable electronic devices. Reducing Ag content, such as Sn98.5Ag1.0Cu0.5 (SAC105), Sn99Ag0.3Cu0.7 (SAC0307), and Sn98.9Ag1.0Cu0.1 (SAC101), improves the non-fragility. This approach often results in an elevated liquidous temperature up to around 227°C. Further improvement has been reported by addition of small amount of Mn, Ti, Bi, Y, Ce, Al, Ni, Zn, Co, Pt, and P.

c. SnAg (+ Bi, +Cu, +In, + dopants)

Lead-free alloys with Bi generally exhibit a lower melting temperature. Furthermore, they are typically better in wetting than other lead-free alloys, presumably due to the low surface tension of Bi (0.376 N/m for Bi versus 0.537 N/m for Sn). The low melting and good wetting features promise a user-friendly soldering process. Addition of Bi to SnAgCu system also refines the intermetallic compound (IMC) grain size and retards the excessive growth of IMC. Addition of small amounts of In reduces the melting temperature and increases the ductility of lead-free alloys.

However, Bi-containing alloys normally exhibit a high rigidity, thus may pose a concern for applications involving a high CTE mismatch or a wide range of service temperatures. In addition, in the presence of lead-contamination, formation of 96°C low melting Bi52Pb30Sn18 ternary eutectic phase can result in early failure at temperature cycling test.

The SnAgBi-containing family is primarily used in Japanese industry, such as Panasonic (SnAgBiCu, SnAgBi, SnAgBiIn), Hitachi (SnAgBi), and Sony (SnAgBiCu). Examples of those alloys supplied mainly in Japanese industry are given below:

Sn97.4Ag1.3Bi0.8Cu0.5 (214-219°C, Nihon Genma)
Sn95.5Ag2.0Bi2.0Cu0.5 (211-221°C, Senju)
Sn94.25Ag2.0Bi3.0Cu0.75 (207-218°C, Senju)
Sn96.0Ag2.5Bi1.0Cu0.5 (214-221°C, Senju, Nihon Almit, Tamura Kaken, Nihon Genma)
Sn95.7Ag2.8Bi1.0Cu0.5 (214-215°C, Nihon Genma)
Sn93.6Ag2.9Bi3.0Cu0.5 (205-216°C, Tamura Kaken)
Sn92.8Ag3.0Bi1.0Cu0.7In2.5 (204-215°C, Senju)
Sn93.3Ag3.0Bi3.0Cu0.7 (206-215°C, Nihon Almit)
Sn91.5Ag3.5Bi2.5In2.5 (Matsushita)
Sn92.5Ag3.5Bi3.0Cu1.0 (208-213°C, Nihon Superior)
Sn91.7Ag3.5Bi4.8 (205-210°C, Sandia National Lab)

d. SnZn (+ Bi)

Eutectic Sn91Zn9 exhibits a melting temperature of 199°C. Although attractive in its low melting temperature, its high surface tension (0.768 N/m for Zn) and high reactivity toward flux

and oxygen prohibit its use for electronic soldering. Addition of Bi, such as Sn89Zn8Bi3 (189-199°C), effectively reduces the surface tension and reactivity, in addition to a further reduction of melting temperature. This enables the SnZnBi alloy to be a viable alternative for lead-free soldering in Japanese industry such as NEC and Panasonic.

However, compared with other lead-free alloys, SnZnBi is still more reactive toward flux and oxygen, therefore is limited in applications. Also, the tendency to form voids on top of CuZn IMC layer on Cu surface further confines this alloy to consumer applications. Other alloys such as Sn86.5Zn5.5Bi3.5In4.5 (174-186°C, Indium) may also be attractive due to a greater melting temperature reduction.

e. BiSn (+Ag)

For BiSn alloys, Bi expands 3.87 vol-% during solidification. Sn contracts, but to a less amount. Thus, BiSn alloys containing more than 47% Bi expand on solidification. Bi58Sn42 (eutectic 138°C) has been used by IBM for wave soldering since more than 30 years ago. Unisys uses this alloy for wave soldering on 50-layer+ mainframe board (1/3-inch-thick), solder pot temperature about 200°C, to reduce thermal shock.

Bi58Sn42 has properties approaching those of Sn63 under most conditions. However, Bi58Sn42 is more sensitive than Sn63 to strain rate. That is, its elongation decreases more rapidly with increasing strain rate. Glazer reported that increased elongation at low strain rates after aging resulted in ductile failure in solder, versus a quasi-brittle fracture at high strain rate. The latter failure mode combines cleavage in Bi-rich phase with fracture at solder/IMC interface.

The ductility of Bi58Sn42 can be improved with addition of Ag, such as Bi57Sn41Ag2. On the other hand, addition of 1% Cu dramatically slowed down coarsening of Bi58Sn42.

2.4.1 Lead-free solder pastes

Solder paste is a mixture of solder powder and flux. The powder size used depends on the applications, with finer powder to be used for finer pitch of PCB assembly. The powder size is defined by IPC as shown in Table 2.4.1.

Type	At least 80% between	At least 85% between
1	150–75 μm	–
2	75–45 μm	–
3	45–25 μm	–
4	–	38–20 μm
5	–	25–15 μm
6	–	15–5 μm
7	–	11–2 μm

Tab. 2.4.1 Particle size distributions of standard solder powders

In the advancing toward miniaturization, flux technology also has to advance in order to cope with the increasing demand on performance.

For a smaller flux/solder paste dot, oxidation of powder, pads, and parts will be more significant due to a shorter oxygen diffusion path. This situation is further aggravated by the increasing surface area per unit volume with decreasing dot size. In other words, the flux fraction which remains to protect the parts from oxidation decreases with increasing miniaturization.

Therefore, either flux with a more efficient oxidation barrier capability or reflow atmosphere with a lower oxygen partial pressure is needed in order to achieve satisfactory soldering results. The relation among soldering performance, oxidation barrier capability, and oxygen partial pressure has been studied by Jaeger and Lee. Less than perfect fluxing will display symptoms such as poor wetting, solder balling, voiding, or poor coalescence.

Besides an improved oxidation barrier capability, the following flux features are also needed with further miniaturization: (1) no-clean, (2) reduced volatile, (3) halide-free, (4) greater fluxing capacity, (5) higher residue resistivity, (6) more resistant to oxidation and charring, (7) lower activation temperature, (8) slower wetting speed when solder begins to melt, (9) less spattering, (10) higher probe penetrability, (11) capability of inducing nucleation of solder upon cooling, and (12) greater slump resistance.

The morphology of solder powder is exemplified in figure 2.4.2. The surface of type 3 powder of Sn63 is fairly smooth, with distinct tin-rich phase (dark phase) and Pb-rich phase (light phase). Sn63 type 7 powder exhibits similar dual phases morphology, with the surface wrinkle being more noticeable under the higher magnification.

Lead-free solder powder often exhibits a rougher surface texture than Sn63 solder powder. In the case of type 3 SAC387 powder, a relatively regular, orange peel-like surface texture is easily recognizable for both alloys. This is mainly attributable to the dendrite formation of beta-tin in the high-tin alloys. The wrinkle formation is also more noticeable for type 6 powder than Sn63. In the case of Bi58Sn42, a distinct Sn-rich (dark phase) and Bi-rich (light phase) two-phase morphology is also observed, with Bi phase being the slightly dominant phase. The crystalline texture of Bi-rich phase results in a bulging formation, as indicated by the 3500X picture of type 5 powder.

The prospects of 10 major lead-free solder alloys for reflow soldering applications are shown in figure 2.4.3. Compatibility of those alloys with a variety of representative flux chemistries was considered essential, and was determined for handling-ability, including shelf life and tack time, and soldering capability, including solder balling, wetting, and solder joint appearance. Results indicated that the control Sn63 was still the most compatible alloy, rated 27.1 out of a full scale of 30 when using warm profile. The primary factor which distinguishes Sn63 from the rest alloys was the soldering performance, particularly the wetting and solder appearance. As to the solder balling, although Sn63 was also the best, it was fairly close to the best lead-free systems.

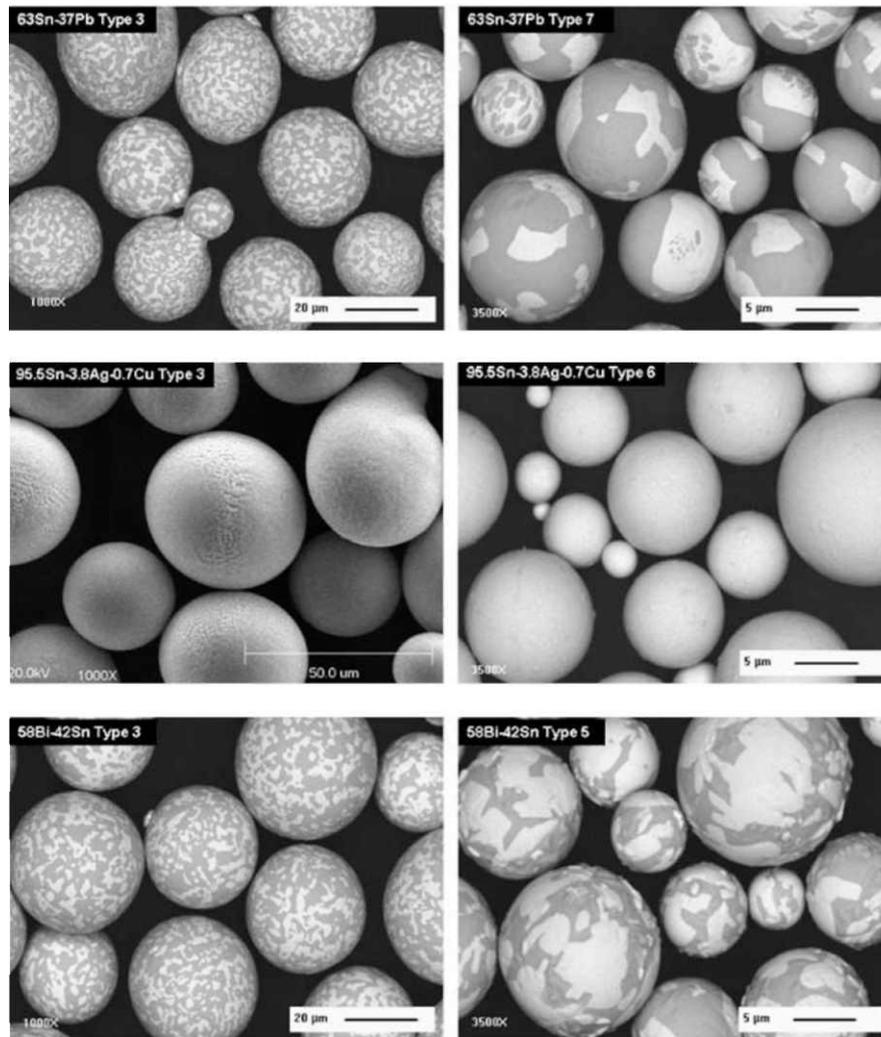


Fig. 2.4.2 BSE pictures of Sn63, SAC387, and Bi58Sn42 solder powder of various sizes

Among the lead-free options, both SnAgBi alloys studied, Sn91.7Bi4.8Ag3.5 and Sn90.5Bi7.5Ag2, turned out to be on the top of lead-free systems, rated 22.9 and 22.8, respectively. This was mainly attributed to the better wetting and solder balling performance. Shelf life and tack time of the SnAgBi systems were also fairly good, while the solder appearance was at best considered average. The six alloys, Sn99.3Cu0.7, Sn95.5Ag3.8Cu0.7, Sn93.6Ag4.7Cu1.7, Sn96.2Ag2.5Cu0.8Sb0.5, Bi58Sn42, and Sn95Sb5, showed fairly comparable performance to each other, ranging from 19.3 to 20.3. In general, the whole group displayed a quite noticeably poorer wetting than SnAgBi systems.

Bi58Sn42 exhibited a fairly poor solder balling performance, but an outstanding solder appearance among lead-free systems. Sn96.2Ag2.5Cu0.8Sb0.5 showed a relatively poor performance in both wetting and solder appearance among these six alloys. Sn96.5Ag3.5, rated 17.1 in compatibility, was ranked below the other alloys described above, mainly due to poor performance in solder balling, and particularly the poor wetting. Sn89Zn8Bi3, rated only 2.2 in compatibility, fell far short in every category when compared with all other alloy systems.

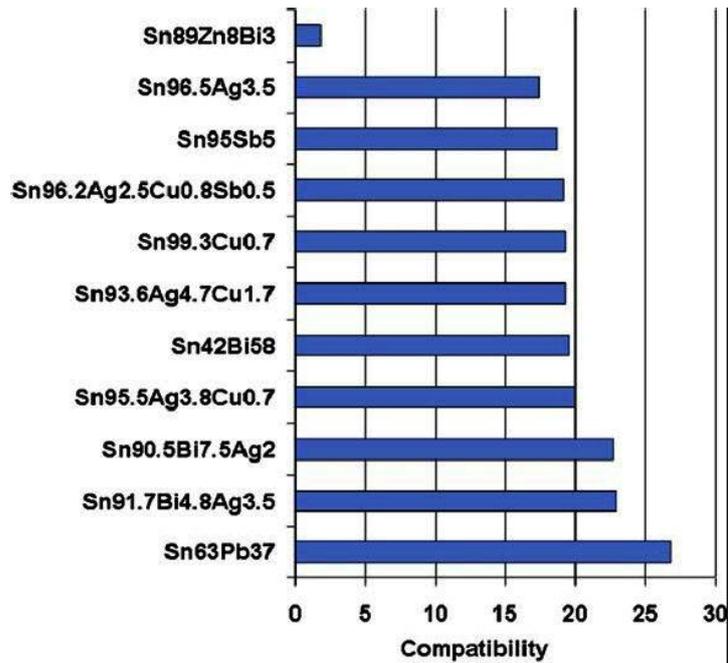


Fig. 2.4.3 Compatibility of alloys with reflow soldering

Obviously, this is attributable to the very reactive nature of zinc, which resulted in excessive oxidation of metal and excessive reaction with fluxes, and consequently an unacceptable performance for solder paste applications. High-tin-content lead-free alloys seemed to display a thicker IMC layer than Sn63 when reflowed. Overall, the reflow compatibility could be ranked in decreasing order as shown below: (1) eutectic SnPb, (2) SnAgBi, (3) SnAgCu, eutectic SnBi, SnAgCuSb, eutectic SnCu, SnSb, (4) eutectic SnAg, (5) SnZnBi.

2.4.2 Lead-free surface finishes

a. Types of lead-free surface finishes

Table 2.4.2 lists the options of lead-free surface finishes for PCBs. The system is categorized per the key element used. Each category is further classified per the type of process and chemistry.

For PCB surface finishes, Organic Solderability Preservative (OSP), Hot Air Solder Level (HASL), immersion Ag (ImAg), Electroless Nickel Immersion Gold (ENIG), and immersion Sn (ImSn) are considered the prevailing options, with estimated global market share for 2007 shown in figure 2.4.3.

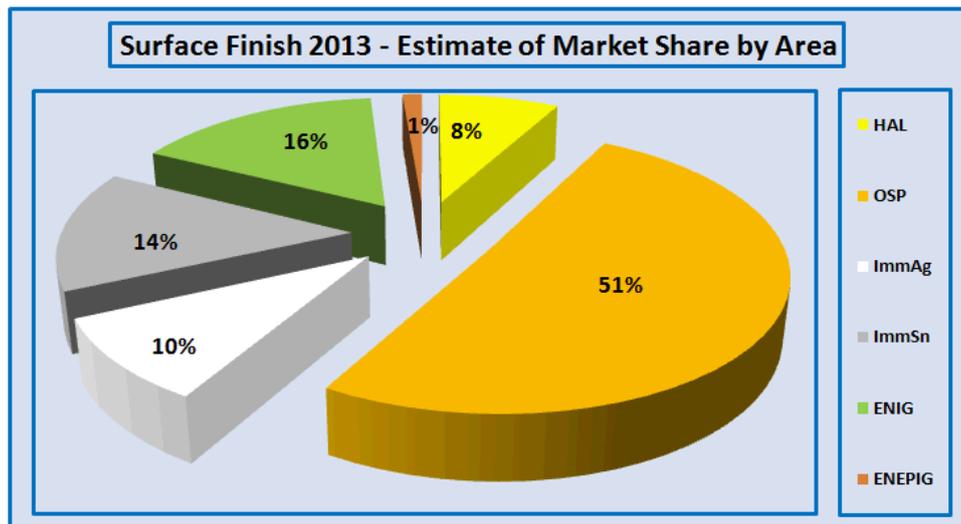


Fig. 2.4.4 Estimated 2013 global market share of PCB surface finishes (Robyn J Hanson, MacDermid, June 25, 2015, SMTA Upper Midwest Expo)

Surface finish system	Finish process & chemistry
Organic Solderability	Benzotriazole
Preservative (OSP)	Imidazole
	Benzimidazole (substituted)
	Preflux (rosin/resin)
Ag	Electroless (immersion, or galvanic) Ag
Au/Ni	Electrolytic Ni/Au, or EG
	Electroless Ni/Electroless (immersion) Au, or ENIG
	Electroless Ni/Electroless (autocatalytic) Au
	Electroless Ni/Electroless (substrate-catalyzed) Au
Bi	Electroless (immersion) Bi
Pd	Electrolytic Pd or Pd-alloys
	Electroless (autocatalytic) Pd
	Electroless (autocatalytic) Pd/Electroless (immersion) Au
Pd/Ni	Electroless Ni/Electroless (immersion) Pd
	Electroless Ni/Electroless (autocatalytic) Pd
	Electroless Ni/Electroless (autocatalytic) Pd/Electroless (immersion) Au
Pd (X)/Ni	Electrolytic Ni/PdCo/Au flash
	(Electroless) Ni/(Electroless) PdNi/Electroless (immersion) Au
Sn	Electrolytic Sn
	Electroless (immersion) Sn
Sn/Ni	Electroless (Modified immersion (autocatalytic) Sn Electrolytic Ni/Electrolytic Sn
SnAg	Electrolytic SnAg
SnBi	Electrolytic SnBi
	Electroless (immersion) SnBi
SnCu	Electrolytic SnCu
SnNi	Electrolytic SnNi

Table 2.4.2 List of lead-free surface finishes. For multi-layer finishes, the sequence of materials starts from the layer on top of base metal

b. Performance of Surface Finishes

The wetting performance of various surface finishes has been evaluated by Horaud et al. via wetting balance. Results showed that the wetting time increased in the following sequence ImAg < ENIG, HASL < ImSn < OSP, while the wetting force decreased in the following sequence ImAg > ENIG > HASL > ImSn >> OSP. On the other hand, the solder spreading displayed the following order HASL > ENIG > ImSn > ImAg > OSP. In general, for properly prepared surface finishes, the solder wettability can be generalized as "metal is better than non-metal, and noble metal is better than non-noble metal". This generalization should be taken with precaution, and HASL should be excluded from this generalization. HASL normally is very easy to wet, since the wetting process involves merely coalescence of molten solder with molten surface finish.

The generalization serves as a guideline and can be challenged by many exceptions due to non-ideal manufacturing conditions. For instance, ENIG may show poor wetting when it suffers serious black pad symptom, while freshly manufactured ImSn can be very good in solderability.

For Pb-free soldering, the type of PCB surface finish affects wetting, bond strength, voiding, aging tolerance and may also affect reliability.

The voiding performance of solder joints is highly affected by the wettability of surface finishes, with poor wettability yielding high voiding. Therefore, tendency of forming large voids decreases in the following sequence OSP (highest in voiding) > HASL > ImAg, ENIG > ImSn. OSP and ImSn are more sensitive to aging. The wettability, bond strength, and voiding of ImSn all deteriorate quickly upon aging. OSP is poorer in both wetting and voiding, but good in bond strength. The pull strength of lead-free QFP solder joints decreases in the following order: OSP > HASL > ImAg > ImSn > ENIG. The sensitivity of OSP toward thermal aging can be reduced by employing new OSP chemistries with higher thermal decomposition temperature.

ENIG is good on wettability, aging tolerance, and voiding. However, it showed the weakest bond strength.

Figure 2.4.5 shows the pull strength of lead-free solder joints on various surface finishes for 50 mil pitch SOICs before and after thermal cycling.

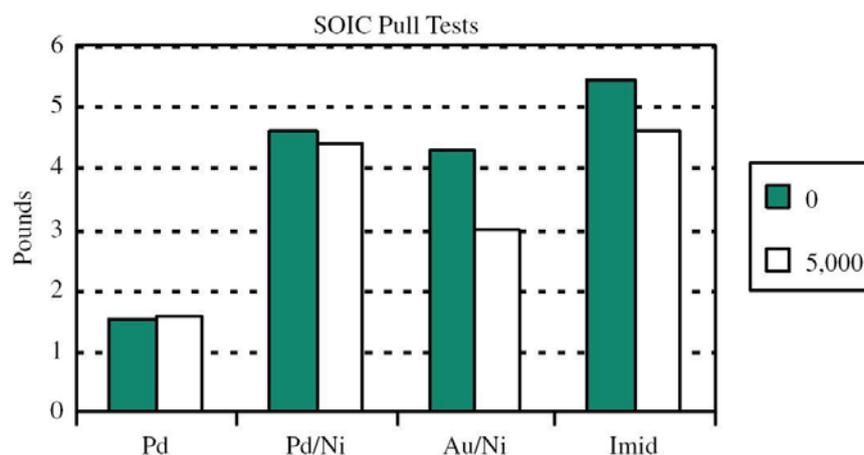


Fig. 2.4.5 Pull strength of lead-free solder joints on various surface finishes before and after thermal cycling test (originally published in SMI 1996)

The low pull strength of Pd finish is attributed to high voiding in solder joints. Thick layer of Pd or Au surface finish is detrimental to reliability and voiding, due to the formation of large quantity of intermetallic compounds PdSn₄ or AuSn₄. In both cases, the volume of the intermetallic compounds formed is approximately 5 times of that of Pd or Au. This is

considerably higher than cases of Cu₆Sn₅, Ni₃Sn₄, or Ag₃Sn, where the volume of the intermetallic compounds is typically less than 2 times of that of surface finish metals. Inclusion of large quantity of intermetallic particles in liquid solder inevitably impedes the escape of voids at soldering, thus results in high voiding and weak bond strength.

ImAg is good in overall performance. Although ImAg is neither the most robust surface finish in terms of solderability nor the highest in joint strength or reliability, it does not have obvious weakness in both features if the finish is properly prepared. As a result, it often becomes the favourable choice thus exhibits the highest CAGR (Compound Annual Growth Rate). However, if not properly prepared, ImAg tends to have Cu cavity under ImAg layer, thus suffers micro-voiding upon soldering. Excessive plating time may even result in discontinuity of circuitry due to complete removal of Cu trace at perimeter of solder mask.

2.4.3 Components for lead-free soldering

Besides the requirement of being lead-free, under European RoHS regulation, the polymeric materials used in electronic devices suffer dual impacts. First of all, a higher soldering temperature is needed due to the higher melting temperature of Pb-free alloys. Secondly, the ban of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) which are commonly used as flame retardants in polymeric materials for packaging and substrates. PBB and PBDE, which include penta-, octa-, and deca-brominated compounds, are banned due to formation of toxic dioxins and furans during combustion.

Temperature Tolerance

JEDEC/IPC J-STD-020D defines the classification temperature for SMD packages, with a higher temperature tolerance demanded for smaller packages, as shown in Table 2.4.3 and Table 2.4.4. In general, the classification temperature for Pb-free process is about 25-40°C higher than that for Sn63 process.

Package thickness	Volume mm ³ < 350	Volume mm ³ 350-2000	Volume mm ³ > 2000
< 1.6 mm	260°C	260°C	260°C
1.6 mm-2.5 mm	260°C	250°C	245°C
> 2.5 mm	250°C	245°C	245°C

Tab. 2.4.3 Pb-free process - classification temperature (T_c)

Package thickness	Volume mm ³ < 350	Volume mm ³ > 350
< 2.5 mm	235°C	220°C
> 2.5 mm	220°C	220°C

Tab. 2.4.4 SnPb eutectic process - classification temperature (T_c)

The thermal stability is comprised of both chemical structural stability and physical structural stability. The chemical structural stability reflects thermal decomposition. The physical structural stability is related to delamination and warpage. In the study of Chung et al., the evolutions of package warpage of two kinds of potential halogen-free compounds during thermal cycling test (TCT) reliability process was monitored. The compound with larger package warpage generated larger cumulate plastic work in solder joint that caused early failure during TCT process.

2.4.4 Substrates for lead-free soldering

The impact of RoHS regulation on substrates is similar to that for plastic component packages. The substrate materials need to be halogen free and capable of surviving a higher process temperature.

Thermal Decomposition

Khan et al. reported that there was a strong indication that high-end products built with current laminate materials would not survive lead-free processes. Problems such as conductive anodic filament (CAF) were aggravated by the higher process temperature. The most critical property upgrade of substrate for lead-free process is probably the resistance toward thermal decomposition. A higher glass transition temperature does not promise a higher decomposition temperature, as shown in Table 2.4.5. Here glass transition temperature and decomposition temperature are two independent properties, and HGHD (High Glass Transition Temperature, High Decomposition Temperature) sample displayed the poorest thermal stability.

Dimensional Stability

Maintaining board dimensional stability is getting more difficult under the elevated lead-free soldering temperature. This is particularly a concern when a large board is held on rails during soldering process. For wave soldering, this board sagging issue may be rectified by employing either a high T_g resin materials, as shown in Table 2.4.6, or by adding a supporting cable under the board. The form stability is also important for flex print circuit (FPC). For fine pitch design, warpage of FPC can easily cause opens, and a high T_g resin is crucial for high yield performance.

Dimensional stability is also critical in preventing pad lifting at annular ring of through hole.

Material	Notation	Glass transition Temp, °C	Decomposition Temp, °C
Low Glass Transition Temp., Low Decomposition Temp.	LGLD	140	320
Low Glass Transition Temp., High Decomposition Temp.	LGHD	140	350
High Glass Transition Temp., Low Decomposition Temp.	HGLD	175	310
High Glass Transition Temp., High Decomposition Temp.	HGHD	175	350

Tab. 2.4.5 Materials with high and low values of T_g and T_d

Resin	T_g (°C)
Standard FR4 epoxies	115–125
Modified FR4 epoxies	120–130
Multi-functional epoxies	140–180
BT epoxies	160–180
Cyanate ester	230–250
Modified polyimides	220–260
Conventional	250–270

polyimides	
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Tab. 2.4.6 Resin type and T_g ($^{\circ}\text{C}$)

Material	x, y axes	z axis
Polyimide E-glass	15–18	45–60
Epoxy E-glass	15–18	45–60
Modified epoxy/aramid	6.5–7.5	95–110
Modified epoxy/quartz	11.0–14.0	55–65

Table 2.4.7 Typical laminate CTEs, in ppm/ $^{\circ}\text{C}$

The coefficient of thermal expansion of copper is 17 ppm/ $^{\circ}\text{C}$, which is considerably lower than that of conventional laminates in the Z-axis direction, as shown in Table 2.4.7. Upon soldering, the laminate expands more than copper, thus causes pad lifting. When using the same soldering peak temperature, use of resin with a higher T_g reduces the adverse impact of high CTE above T_g , α_2 . This effectively reduces the mismatch in dimension, and consequently alleviates the pad lifting problem.

2.4.5 Reliability of Lead-Free Solder Joints

The two most important types of reliability of lead-free solder joints for electronic devices are temperature cycling and drop test performance. The impact of materials, processes, and environment on the reliability will be discussed below. Since the reliability is governed by the microstructure, it is crucial to know the microstructure of solder joints first, particularly the intermetallic compounds (IMC) formed in the joints.

Microstructure

The microstructure of tin-silver-copper solders, such as SAC387, is shown in Figure 2.4.6, where a number of short rod-like bright Ag_3Sn particles and some small dark grey Cu_6Sn_5 particles are dispersed in the tin matrix between the grey tin dendrites. Few large Cu_6Sn_5 particles can also be seen randomly dispersed. At Ag content above approximately 2.5 wt%, large Ag_3Sn platelet formation may also be found.

At reflow, upon cooling, the large Ag_3Sn platelets may form first, followed by tin dendrites formation from liquid solder. Upon further cooling, small Ag_3Sn and Cu_6Sn_5 particles further precipitate out in between tin dendrite globes.



Fig. 2.4.6 Scanning electron micrograph of cross-sectioned SAC387 solder reflowed on Cu

For eutectic SnAg and SnCu alloys, similar small rods of Ag_3Sn particles and Cu_6Sn_5 particles are formed respectively in between tin dendrites.

2.4.6 Solder Joint Intermetallics

a. SAC on Cu-Based Substrate

For SAC solder, the intermetallics formed at interface on Cu are Cu_6Sn_5 near solder side and Cu_3Sn near Cu side. For wave soldering, the IMC thickness is very thin, often around or smaller than 0.1mm and is barely discernible. For reflow soldering, the IMC thickness is typically around 2mm, with Cu_6Sn_5 as the dominant layer. Upon aging, Cu_3Sn layer grows quickly and becomes comparable to that of Cu_6Sn_5 layer, as shown in Figure 2.4.7. The IMC thickness may be as high as 5 mm for some BGA joints. Kao reported that as little as 0.1% Ni addition is able to hinder Cu_3Sn formation on Cu.

b. SAC on Ni-Based Substrate

The IMC formed on NiAu is more complicated than that on Cu. Kao studied the effect of Cu content in solder on IMC structure on Ni-based substrates, as shown in Table 2.4.8. For joints with small solder volume, the Cu content decreased readily with growth of IMC. This resulted in shifting of equilibrium phase at interface, and eventually could cause the massive spalling of IMC layer.

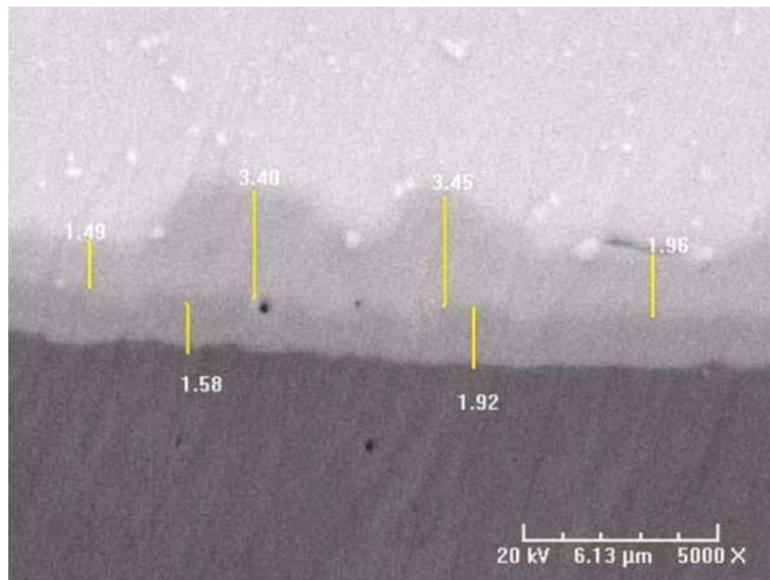


Fig. 2.4.7 SAC305 solder joint on Cu after aging at 150°C for 10 days. IMCs formed at interface, with Cu_6Sn_5 near solder side and Cu_3Sn near Cu side

Cu content in solder	IMC formed
< 0.3 wt%	Only $(\text{Ni,Cu})_3\text{Sn}_4$ forms
0.4-0.5 wt%	Both $(\text{Ni,Cu})_3\text{Sn}_4$ and $(\text{Cu,Ni})_6\text{Sn}_5$ form
> 0.5 wt%	$(\text{Cu,Ni})_6\text{Sn}_5$ forms

Tab. 2.4.8 Effect of Cu content on IMC structure formed on Ni-based substrates, if the supply of Cu is not an issue

Lu et al. studied the effect of Cu content in solder on IMC structures formed between Cu-based substrate and Electroless Ni immersion Au (ENIG) substrate. The results can be illustrated with Figure 2.4.8. The IMC on Cu-substrate remained as $(\text{Cu,Ni})_6\text{Sn}_5$. However, the IMC composition on ENIG substrate varied with increasing Cu content in solder. At 0% Cu concentration, multiple layers of IMC formed on Ni surface. With increasing Cu concentration, $(\text{Ni,Cu})_3\text{Sn}_4$ changed to $(\text{Cu,Ni})_6\text{Sn}_5$, and NiPSn and $\text{Ni}_3(\text{Sn,P})$ gradually merged and eventually vanished. At 0 to 0.5 wt% Cu, no Ag_3Sn plates were observed in any locations of the solder joints at time zero. On the other hand, high Cu led to flourishing growth of CuSn IMCs. The latter promotes the growth of Ag_3Sn platelets.

The TEM (transmission electron microscopy) image of the interfacial structure of SnAgCu and Au/Ni(P)/Al joint after 5 reflows was examined. Within the NiSnP layer with a thickness of 0.1mm, micro-voids were formed due to diffusion of Sn away from this layer.

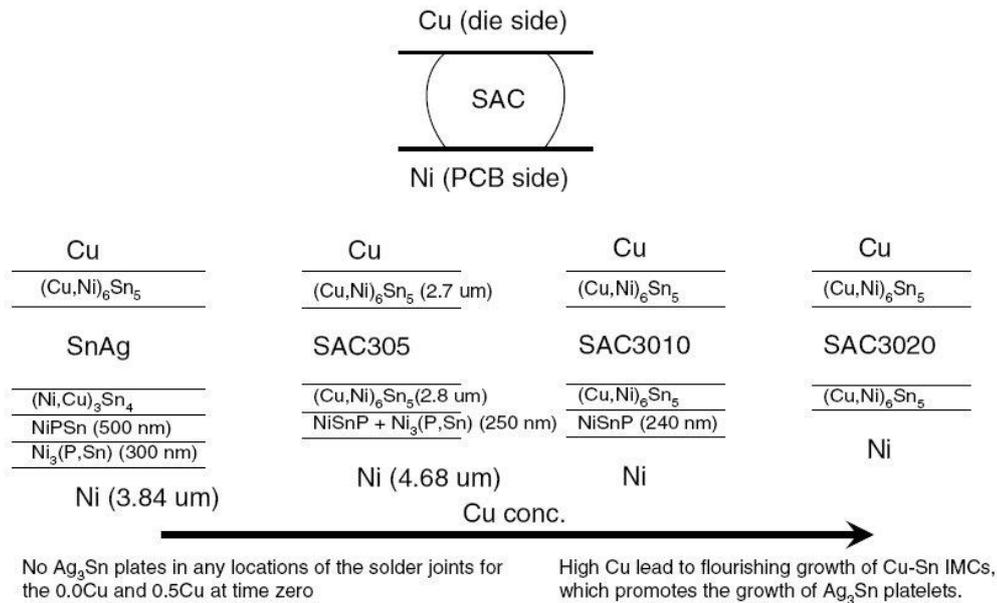


Fig. 2.4.8 Effect of Cu content in solder on IMC structure of solder joints formed between Cu-based substrate and ENIG substrate

c. IMC Growth

Song et al. studied the effect of thermal aging at 150°C on IMC formation rate of lead-free solders on OSP and ENIG, with results shown in Figure 2.4.9. OSP exhibited a higher IMC growth rate than ENIG, mainly attributable to the higher diffusion rate of Cu than Ni. On OSP, SAC405 showed a lower growth rate than Sn96.5Ag3.5 (SA), presumably due to the retardation of Cu substrate diffusion in the presence of Cu in solder. On ENIG, SAC405 also appeared to be slightly lower in IMC growth rate than SA.

Xu et al. compared the effect of isothermal aging, temperature cycling, and thermal shock on IMC growth rate for SAC387/NiAu BGA specimen. The test conditions were 125°C for isothermal aging, -40 ~ 125°C, 15 min. high temperature (T) dwell, 1 hr/cycle for temperature cycling (TC), and -55 ~ 125°C, 5 min. high T dwell, 17 min/cycle for thermal shock (TS), respectively. For TC and TS tests, IMC thickness was measured at 500, 1000, 1500, and 2000 cycles. Results are shown by plotting IMC thickness against square root of time (hours), as shown in Figure 2.4.10. As expected, IMC thickness increased with increasing testing time. It is interesting to note that IMC growth rate displayed the following order: TS > TC > isothermal aging, despite the fact that isothermal aging had the longest exposure time at 125°C during the same testing time span. Apparently, thermal stress played a more dominant role than 125°C conditioning in expediting IMC growth, and a higher thermal stress resulted in a higher IMC growth rate.

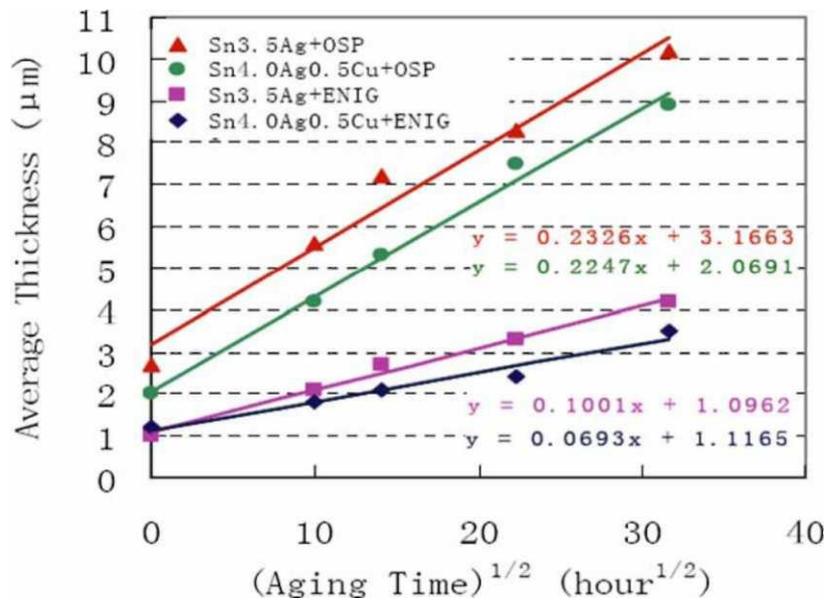


Fig. 2.4.9 Correlation between IMC thickness and 150°C aging time (Cu-Sn phase in both SA and SAC405 on OSP; Ni-Cu-Sn phase in SAC405 on ENIG; Ni-Sn phase in SA on ENIG) (IEEE copyright)

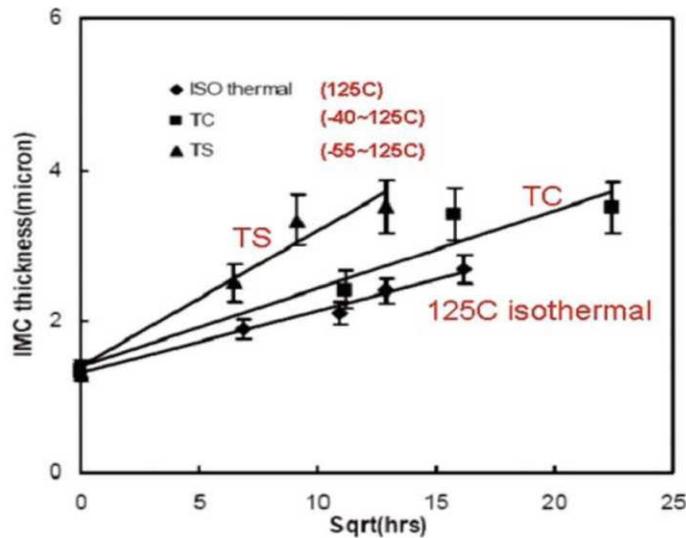


Fig. 5.21 Comparison of IMC thickness: TC, TS, Isothermal Aging, SAC387/Ni-Au couple (IEEE copyright) [82]

Fig. 2.4.10 Comparison of IMC thickness: TC, TS, Isothermal Aging, SAC387/Ni-Au couple (IEEE copyright)

d. Temperature Cycling

The reliability of solder interconnects formed with SAC397 and SA was determined by Osterman et al. using CLCC (ceramic leadless chip carrier) assemblies subjected to various thermal cycling conditions. The test results indicated:

- (1) At the lower cyclic mean temperatures, Pb-free solders showed better reliability than SnPb solder.
- (2) At the highest tested cyclic mean temperature which had a cyclic peak temperature of 125°C, SnPb solder outperformed the Pb-free solders.
- (3) Effect of the dwell time decreased with the increasing cyclic mean temperature.
- (4) At temperatures under 100°C regardless of dwell time, Pb-free solder was more reliable than SnPb solder.
- (5) Reliability of the Pb-free solders showed much stronger dependence on the cyclic medium temperature than the SnPb solder.

2.4.7 Effect of Alloy Composition

Solder composition has a great impact on temperature cycling performance. Terashima et al. reported that in Sn-xAg-0.5Cu system, the 50% failure rate for 1, 2, 3, and 4% Ag content alloys occurred at approximately 305, 375, 545, and 605 cycles, respectively. In other words, a decrease of Ag content from 4 to 1% decreased the thermal fatigue life (50% failure) of flip chip joints on Cu pads by a factor of about 2. All alloys tested had 0.5% Cu, and the test cycle was -40/125°C, 10 min. dwell. The fracture was reported to be a mixed mode, trans-granular and inter-granular, independent of the silver content. The positive effect of Ag content on thermal fatigue life was attributed to the reinforcement of Ag₃Sn IMC particles. A higher Ag₃Sn concentration resulted in a more rigid solder, partly through reinforcement effect, partly through refining the Sn grain size. Presence of large amounts of Ag₃Sn IMC particles also suppressed microstructural coarsening more effectively, thus maintained a higher fatigue resistance. Increase in Cu content may have a similar effect through reinforcing power of Cu₆Sn₅ IMC particles. However, this approach could result in a wider pasty range by raising the liquidus temperature. For instance, at 4 wt% Cu content, the liquidus should be higher than 300°C, therefore may impose challenge on soldering process.

The fragility of lead-free solder joints was attributed to the higher hardness of lead-free solders. Upon impact, the shock energy could not be dissipated by the ductility of solder, thus causing the cracking of the weakest link IMC layer at interface. For SAC alloys, both Ag and Cu would increase the hardness of solder due to formation of Ag₃Sn and Cu₆Sn₅ IMC particles. Since Cu content not only is relatively low, but also is desired in order to prevent IMC spalling on Ni surface upon aging, reducing Ag content turns out to be the logical shortcut to reduce the hardness of SAC solders. Therefore, in drop test, SAC105 BGA joints were reported by Liu et al. to be about 5 times better than SAC387 and SAC305 on electroplated NiAu substrate, although they were still not as good as Sn63, as shown in Figure 2.4.11.

The effect of Cu content on fragility is not as straight forward as Ag. Although decrease in Cu content is expected to reduce the fragility of joints due to reduction in hardness, increase the Cu content to 2 wt% was found to transform the solder into a ductile material, and consequently eliminated the fragile failure mode of Sn95Ag3Cu2 solder joints.

Besides varying Ag and Cu content, adding small amounts of certain elements into solder was also effective in reducing the fragility of SAC solder joints. Liu et al. reported Mn, Ti, Ce, Bi, and Y were effective in reducing the fragility of SAC solder joints, with Mn and Ti being the most effective. While SAC-Mn system was found to outperform Sn63 and SAC105 in most incidences, SAC-Ti was observed to have the best performance overall for joints on ENIG/OSP, NiAu/OSP, and OSP/OSP surface finishes. The superior performance of SAC-Ti was attributed to (1) the increased grain size and dendrite size, therefore reduced hardness of solder, (2) inclusion of Ti in the IMC layer, and (3) reduced IMC layer thickness. Amagai et al. found addition of 0.2 wt% In and 0.04 wt% Ni improved drop test performance by 20%. Co, Ni and Pt were dissolved in IMC, which did not increase IMC grain size and thickness significantly after 4 times solder reflow processes. Upon pull test, the fracture occurred mainly in bulk solder instead of at interface.

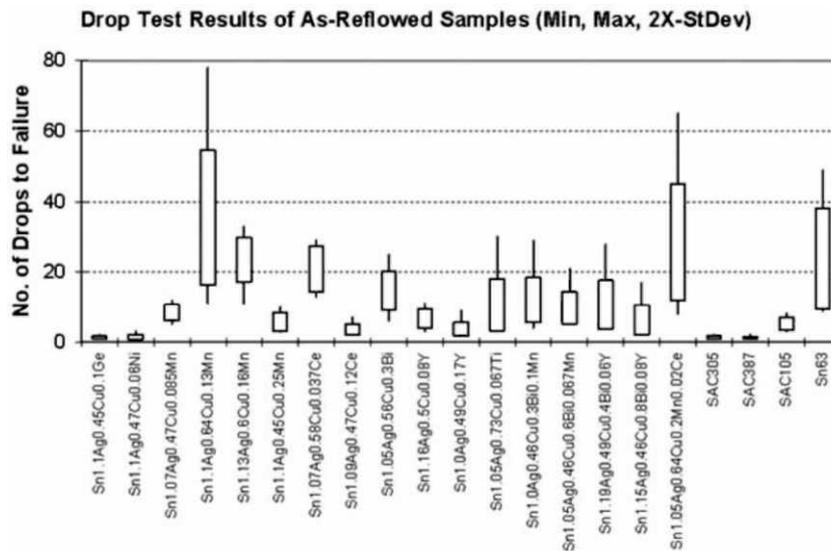


Fig. 2.4.11 Drop test results of reflowed samples. The thin lines represent minimum and maximum values; the box represents the standard deviation, the midpoint being the mean value

The reduction of fragility of the above approaches was conducted by modifying low Ag SAC systems. As shown in Figure 2.4.11, low Ag typically results in a compromise in thermal cycle fatigue resistance. Huang et al. investigated alloys exhibiting both high thermal fatigue and low fragility properties. Their results indicated that, for high Ag SAC alloys, adding Al 0.1-0.6% to SAC alloys was most effective in softening, and brought the yield strength down to the level of SAC105 and SAC1505, while the creep rate was still maintained at SAC305 level, as shown in Figure 2.4.12.

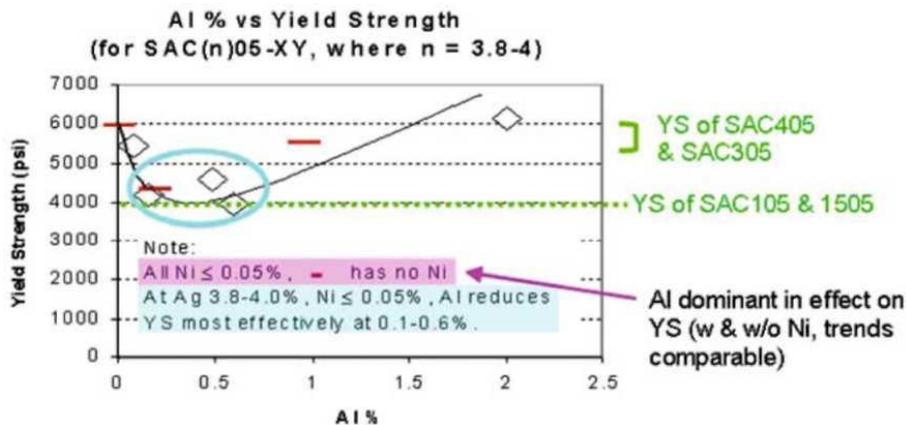


Fig. 2.4.12 Effect of Al addition on yield strength of SAC(n)05-XY

Although SAC solder joints have been satisfactory versus SnPb joints in thermal cycling test, the fragility of solder joints was recognized later as the unexpected weakness of lead-free alloys.

		Board finish	
		Cu	Ni
Component finish	92Sn8Pb	5081	3250
	Sn	4000	1595

Tab. 2.4.9 Number of cycles to first failure versus board/component finish

2.4.8 Effect of Surface Finish

Zbrzeznya et al. studied the effect of surface finish on the accelerated temperature cycling performance of SAC387 solder joints for chip resistors. The board finishes tested included Cu (immersion Ag and HASL) and Ni (ENIG), while the component finishes tested included Sn92Pb8 and 100% Sn. Results from Table 2.4.9 showed the joints to copper on board exhibited a significantly higher number of cycles to first failure than the joints on nickel on board. On the other hand, component finish Sn92Pb8 was moderately better than Sn-finish.

The significantly better reliability of the copper joints can be explained in terms of the copper content in the bulk. On Cu board, dissolution of Cu pad caused an enriched Cu content of joints, hence joints with refined grain size due to presence of abundant Cu_6Sn_5 IMC particles at grain boundary. This eventually resulted in a longer thermal cycling life. SAC387 joints on Ni board were depleted with Cu due to formation of $(Cu,Ni)_6Sn_5$ IMC layer at joint interface, thus suffered a coarser grain size, and consequently a shorter cycling life.

The surface finish has a significant effect on fragility of lead-free solder joints. Arra et al. studied drop test performance of SAC396 solder joints, observed the drop number for NiPd, Sn85Pb15, and Sn98Bi2 to be 10, 13, and 20, respectively. In another study, the drop number was found to be independent of the joint strength by variation of lead coating, as shown in Table 2.4.10.

Lead coating	Average pull force (N)	Average number of drop cycles to drop off
Ni/Pd/Au	23.3	3.5
Sn98Bi2	20.0	9.5
Sn85Pb15	17.3	6.6
Sn	14.3	5.2

Tab. 2.4.10 Solder joint strength versus drop number for various lead coatings

Darveaux et al. studied the failure mode of solder joints on various PCB surface finishes in pull test. Results indicated (1) more reflow heat caused more brittle failure on Cu than on NiAu, (2) propensity toward brittle failure decreased in the following order: ImSn > ENIG > OSP > NiAu.

Song et al. also studied the failure mode of SAC BGA ball on OSP and ENIG via pull test. Their results show that OSP was more prone to brittle failure than ENIG. The brittle failure on the ENIG was induced by weak joint between the IMC and the Ni layers and the brittleness of IMC itself, as shown in Figure 2.4.13. The brittle failure on the OSP pad was induced mainly by weak joint of Cu_6Sn_5 and Cu_3Sn IMC phases.



Fig. 2.4.13 Failure site of SAC solder joints on Ni and Cu in pull test

2.4.9 Conclusions

Materials for lead-free soldering will be more and more used, especially SAC. The soldering processing window is narrower than that of Sn63, mainly due to the elevated melting temperature of SAC solder and the limited high temperature tolerance of components and board. The reliability of lead-free solder joints is acceptable for thermal cycling performance. However, the fragility of joints remains a concern, although significant improvement has been accomplished.