Fluxul de operații

“CAE-CAD-CAM” pentru dezvoltarea modulelor electronice

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Demonstraţie în OrCAD

Modulul electronic propus ca exemplu poate fi utilizat pentru afişarea digitală a tensiunii şi curentului unei surse de alimentare de laborator existente, care nu dispune de acest afişaj.
Schema 1 - Datele inițiale pentru proiectarea modulului PCB
First of all some words about the working principle of the circuit.

- The schematics from fig. 2 will not be used, but it suggests a required intervention in the existing power supply.
- The main change is the insertion of the series (shunt) resistor R6.
- The connection of the module with the power supply will be assured by the connector pins A-F.
The switch between the U/I display mode is done by the DPDT (Double Pole Double Throw) switch S1 (not included in our PCB).

For voltage measurement the voltage applied to IC1 is divided by the group R1-P4 in a quotient 1:100. The decimal point of LD3 and the LED “V” are lit on, the display resolution is 0,1 V.

For current measurement the voltage drop at R6, is applied directly at HI-LO terminals of the DAC circuit IC1. In this case there are two possible scale connections (a) - 0÷9,99 A or connection (b) - 0÷0,999 A. In these cases the shunt resistor must have the values 0.1 Ω, respectively 1 Ω.

The circuit has 4 adjustment points:
• P1 null point adjustment for current domain
• P2 full scale calibration for current
• P3 null point adjustment for voltage domain
• P4 full scale calibration for voltage

The adjustments must be done in this order.
Demonstration of design flow in OrCAD

Înainte de orice activitate CAD va trebui să răspundem la câteva întrebări:

- Cum va arăta carcasa (cutia)?
- Cum este alimentat circuitul?
- Câte plăci-module PCB sunt necesare?
- Câte straturi trebuie să aibă plăcile?
- Câţi conectori se vor utiliza?
- Se vor utiliza componente SMD sau THT? Etc.

Pentru a răspunde la unele întrebări trebuie să privim proiectul CAD în ansamblu, ca parte a unui proiect de construcție a unui aparat electronic.
PRIMA ACTIVITATE: Adunarea de informații despre componente

Surse: Cataloge ale distribuitorilor, foi de catalog ale fabricanților accesibile pe Web, etc.
C1 Metalized film capacitor

C2, C3 Multilayer ceramic capacitors MCC

<table>
<thead>
<tr>
<th>Case</th>
<th>L max.</th>
<th>H max.</th>
<th>e max.</th>
<th>ø ± 0.02</th>
<th>Observations</th>
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<tr>
<td>01</td>
<td>7.5 (0.295)</td>
<td>6.5 (0.256)</td>
<td>2.5 (0.098)</td>
<td>0.5 (0.020)</td>
<td>1nF ≤ C≤ 220nF</td>
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<tr>
<td>02</td>
<td>7.5 (0.295)</td>
<td>8.0 (0.315)</td>
<td>3.2 (0.126)</td>
<td>0.5 (0.020)</td>
<td>12nF ≤ C≤ 330nF</td>
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<tr>
<td>05</td>
<td>7.5 (0.295)</td>
<td>12.0 (0.472)</td>
<td>6.0 (0.236)</td>
<td>0.5 (0.020)</td>
<td>560nF ≤ C≤ 2.2μF</td>
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<tr>
<td>06</td>
<td>7.5 (0.295)</td>
<td>9.6 (0.378)</td>
<td>6.0 (0.236)</td>
<td>0.5 (0.020)</td>
<td>47nF / 400V</td>
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<tr>
<td>07</td>
<td>7.5 (0.295)</td>
<td>8.0 (0.315)</td>
<td>5.0 (0.197)</td>
<td>0.5 (0.020)</td>
<td>27nF ≤ C≤ 1μF</td>
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C5215
Keramik-Vielschicht-Kondensatoren, lose
Keramikart: NPO
Rastertaug: 0,08 mm
Hersteller: TPC, Kemet

Abmessungen

<table>
<thead>
<tr>
<th>L</th>
<th>h</th>
<th>e</th>
<th>ø</th>
<th>RM</th>
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<tr>
<td>[mm]</td>
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<td>[mm]</td>
<td>[mm]</td>
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<tr>
<td>3.8</td>
<td>5.8</td>
<td>2.5</td>
<td>0.5</td>
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CV_PFN-5
C4 Aluminium Electrolytic Capacitor

C6380

Miniatur-Elektrolyt-Kondensatoren, radiale Anschlüsse, gequert und lose
Temperaturbereich: -40 ... 105 °C
Nennspannung: 25 V DC

<table>
<thead>
<tr>
<th>CSHT_</th>
<th>C [μF]</th>
<th>U_N [V]</th>
<th>I_R [mA]</th>
<th>D [mm]</th>
<th>L [mm]</th>
<th>RM [mm]</th>
<th>d [mm]</th>
<th>Lieferform</th>
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<td>0022/25</td>
<td>22</td>
<td>25</td>
<td>47</td>
<td>5</td>
<td>11</td>
<td>5,0</td>
<td>0,5</td>
<td>gegurtet</td>
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<tr>
<td>0100/25</td>
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<td>25</td>
<td>110</td>
<td>6,3</td>
<td>11</td>
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<tr>
<td>0220/25</td>
<td>220</td>
<td>25</td>
<td>190</td>
<td>8</td>
<td>11</td>
<td>5,0</td>
<td>0,6</td>
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<td>0470/25</td>
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<td>25</td>
<td>340</td>
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<td>16</td>
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<tr>
<td>1000/25</td>
<td>1000</td>
<td>25</td>
<td>610</td>
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<td>2200/25</td>
<td>2200</td>
<td>25</td>
<td>930</td>
<td>13</td>
<td>26</td>
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<td>0,8</td>
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<td>25</td>
<td>1420</td>
<td>18</td>
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<td>lose</td>
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<tr>
<td>6800/25</td>
<td>6800</td>
<td>25</td>
<td>1710</td>
<td>18</td>
<td>42</td>
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<td>0,8</td>
<td>lose</td>
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</table>

C = Nennkapazität, U_N = Nennspannung DC, I_R = Ripple Current (85 °C, 120 Hz)
0.125W Metal Film Resistors

<table>
<thead>
<tr>
<th>Technical Specification</th>
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<tr>
<td>Rated dissipation at 70 °C</td>
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<tr>
<td>Tolerance</td>
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<tr>
<td>Temperature coefficient</td>
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<tr>
<td>Limiting element voltage</td>
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<tr>
<td>Ambient temperature range</td>
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</tbody>
</table>

R1-R5 Metal film resistors

P1-P4 Multi Turn Cermet Trimmers
LD1-LD3 7 Segments LED Display

CATHODE\textsubscript{a} 1
CATHODE\textsubscript{f} 2
COMMON ANODE 3
NO PIN 4
NO PIN 5
CATHODE D.P. 6
CATHODE\textsubscript{e} 7

14 COMMON ANODE
13 CATHODE\textsubscript{b}
12 NO PIN
11 CATHODE\textsubscript{g}
10 CATHODE\textsubscript{c}
9 NO CONNECTION
8 CATHODE\textsubscript{d}

W. 12.7, H. 19.05, D. 6.35 (ex. pins)
Pin spacing 2.54, Row spacing 7.62

LD1-LD3 7 Segments LED Display

D1-D2 LEDs for “Volts” or “Amps” Display

Short Lead Cathode
L. (Body) 8.8 Dia. 5 Lead Pitch 2.54 Leads 0.45sq.
**A3132**

Brückengleichrichter 1,5 A, glaspassiviert
Gehäuse: rund

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**FAGOR**

---

**Technische Daten**

<table>
<thead>
<tr>
<th>Type</th>
<th>$V_{RWM}$</th>
<th>$V_{RMS}$</th>
<th>$V_F$</th>
<th>$I_{F(AV)}$</th>
<th>$I_R$</th>
<th>$T_J$</th>
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<tr>
<td></td>
<td>[V]</td>
<td>[V]</td>
<td>[V]</td>
<td>[A]</td>
<td>[mA]</td>
<td>[°C]</td>
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<td>100</td>
<td>40</td>
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<td>1,5</td>
<td>10</td>
<td>-40...+150</td>
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<td>200</td>
<td>80</td>
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<td>1,5</td>
<td>10</td>
<td>-40...+150</td>
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<td>380</td>
<td>1,1</td>
<td>1,5</td>
<td>10</td>
<td>-40...+150</td>
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</tbody>
</table>

$V_{RWM}$ = Max. peak working voltage, $V_{RMS}$ = Recommended input voltage, $V_F$ = Max. forward voltage drop per element at $I_F = 1,5$ A, $I_{F(AV)} = 15$ A. $I_R$ = Max. reverse current per element. $T_J$ = Operating temperature range.
SW1 SPDT Switch

Top Actuated
Silver Contacts
Shorting Contacts
Terminals with .100" Spacing

Through-Hole

J1 Jack female connector

J2 In-line pins connector

PG203JN

G5224 Stiftleisten gerade 1-reihig RM2,54

<table>
<thead>
<tr>
<th>Artikel</th>
<th>Artikelbezeichnung</th>
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<td>ASLO50Z</td>
<td>Stift. 50pol gerade 1R Zinn</td>
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<td>ASLO56TG</td>
<td>Stift. 50pol gerade 1R Teilgold</td>
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<td>ASLO56G</td>
<td>Stift. 50pol gerade 1R Gold</td>
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<table>
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<td>2.54</td>
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<tr>
<td>0.635</td>
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On-None-On Single Pole Models

Inch .100" with Gray Base
BC546; BC547 NPN general purpose transistors

Fig. 1 Simplified outline (TO-92; SOT54) and symbol.

T4, T5 small signal transistors

BC636; BC638; BC640
PNP medium power transistors

Fig. 1 Simplified outline (TO-92; SOT54) and symbol.

T1- T3 medium power transistors
CA3161

BCD to Seven Segment Decoder/Driver

Features
- TTL Compatible Input Logic Levels
- 25mA (Typ) Constant Current Segment Outputs
- Eliminates Need for Output Current Limiting Resistors
- Pin Compatible with Other Industry Standard Decoders
- Low Standby Power Dissipation: 18mW (Typ)

Description
The CA3161 is a monolithic integrated circuit that performs the BCD to seven segment decoding function and features constant current segment drivers. When used with the CA3162 A/D Converter the CA3161 provides a complete digital readout system with a minimum number of external parts.

Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TEMP RANGE (°C)</th>
<th>PACKAGE</th>
<th>PKG. NO.</th>
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<tr>
<td>CA3161</td>
<td>0 to 70</td>
<td>16 Ld PDIP</td>
<td>816.3</td>
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</tbody>
</table>

U1 A/D Converter

CA3162

A/D Converters for 3-Digit Display

Features
- Dual Slope A/D Conversion
- Multiplexed BCD Display
- Ultra Stable Internal Band Gap Voltage Reference
- Capable of Reading 99mV Below Ground with Single Supply
- Differential Input
- Internal Timing - No External Clock Required
- Choice of Low Speed (4Hz) or High Speed (96Hz) Conversion Rate
- "Hold" Inhibits Conversion but Maintains Delay
- Overrange Indication
- "EEE" for Reading Greater than +999mV, "+" for Reading More Negative than -99mV When Used With CA3161E

Description
The CA3162E and CA3162AE are monolithic A/D converters that provide a 3 digit multiplexed BCD output. They are used with the CA3161E BCD-to-Seven-Segment Decoder/Driver and a minimum of external parts to implement a complete 3-digit display. The CA3162AE is identical to the CA3162E except for an extended operating temperature range. The CA3161E is described in the Display Drivers section of this data book.

Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>TEMP RANGE (°C)</th>
<th>PACKAGE</th>
<th>PKG. NO.</th>
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<tr>
<td>CA3162E</td>
<td>0 to 70</td>
<td>16 Ld PDIP</td>
<td>816.3</td>
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</tbody>
</table>

U2 BCD Decoder

Pinout Diagram
U3 Voltage Regulator

L7800 SERIES

POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 1.5 A
- OUTPUT VOLTAGES OF 5; 5.2; 6; 8; 8.5; 9; 12; 15; 18; 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSITION SOA PROTECTION

DESCRIPTION
The L7800 series of three-terminal positive regulators is available in TO-220 TO-220FP TO-3 and D²PAK packages and several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)

TO-220 & TO-220FP D²PAK TO-3
NEXT STEP:

Realization of the Schematic Drawing

File → New Project
<table>
<thead>
<tr>
<th>Art.</th>
<th>Qty.</th>
<th>Ref.</th>
<th>Value</th>
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<th>PCB Footprint (Library)</th>
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<tr>
<td>1</td>
<td>1</td>
<td>B1</td>
<td>B40C1000</td>
<td>BRIDGE/DISCRETE</td>
<td>BR_40– new created</td>
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<tr>
<td>2</td>
<td>1</td>
<td>C1</td>
<td>270n</td>
<td>CAP/DISCRETE</td>
<td>RAD/.300X.125/LS.200/.031 (TM_RAD)</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>C2,C3</td>
<td>100n</td>
<td>CAP/DISCRETE</td>
<td>RAD/.250X.125/LS.200/.031 (TM_RAD)</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>C4</td>
<td>470u/25V</td>
<td>CAP POL/DISCRETE</td>
<td>CPCYL/D.400/LS.200/.034 (TM_CAP_P)</td>
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<tr>
<td>5</td>
<td>1</td>
<td>D1</td>
<td>Ampers</td>
<td>LED/DISCRETE</td>
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<tr>
<td>6</td>
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<td>CONN PCB 2-R/CONNECTOR</td>
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<td>P1</td>
<td>50k</td>
<td>TRIM- new created</td>
<td>VRES16 (VRES)</td>
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<td>82R</td>
<td>R/DISCRETE</td>
<td>AX/.350X.100/.031 (TM_AXIAL)</td>
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<td>15k</td>
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<td>LM7805</td>
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Some parts (symbols) or/and footprints must be created
### Capture CIS - Properties Editor

#### Preparing Capture for transfer

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<td>I12493</td>
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<td>I00237</td>
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<tr>
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<td>LD2</td>
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</tr>
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<td>R4</td>
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<td>I03960</td>
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<td>I10265</td>
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<td></td>
<td>AXI/350X.100/0.031</td>
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<tr>
<td>SW KEY-SPDT</td>
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<td>DEFAULT</td>
<td>I12643</td>
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<td>SPDT</td>
</tr>
</tbody>
</table>

---

*Image: Screen capture of Capture CIS - Properties Editor window with data for various components and their properties.*

*Text: Preparing Capture for transfer - Properties Editor.*
The correspondence symbol-footprint (SCM-PCB) at Netlist transfer in Orcad.

<table>
<thead>
<tr>
<th></th>
<th>Schematic Capture</th>
<th>PCB Layout</th>
<th>Obs.</th>
</tr>
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<tr>
<td>1</td>
<td>Pin name 1 2</td>
<td>Pin name 1 2</td>
<td>Correspondence realized correctly.</td>
</tr>
<tr>
<td>2</td>
<td>Pin name A K</td>
<td>Pin name A K</td>
<td>Correspondence realized correctly.</td>
</tr>
<tr>
<td>3</td>
<td>Pin name A K</td>
<td>Pin name 1 2</td>
<td>Correspondence realized correctly.</td>
</tr>
<tr>
<td>4</td>
<td>Pin name A K</td>
<td>Pin name 1 2</td>
<td>No correspondence found. Error at AutoECO run.</td>
</tr>
<tr>
<td>5</td>
<td>Pin name 1 2</td>
<td>Pin name 1 2</td>
<td>Attention! The correspondence is found, but with wrong results. The field “Pin number” has priority.</td>
</tr>
<tr>
<td>6</td>
<td>Pin name 1 2</td>
<td>Pin name 1 2</td>
<td>No correspondence found. Error at AutoECO run. *= any character different from those found in field “Pin name” from Layout. (1 resp. 2)</td>
</tr>
</tbody>
</table>

Recommendation:
- Use numbers, majority of Layout libraries use numbers.
- Exceptions: TM_CAP_P, TM_DIODE.
- Modify symbols (parts) in libraries not in Schematic Page.
- Take your time and think twice!
TRANSFER TO LAYOUT

- The field “PCB Footprint” must be filled in (correctly).
- DRC Verification.
- Postprocessing: Netlist, Bill of Materials, Printing.
- Nets verification - Not a CAD activity!!!
Import of Netlist in Layout Block:

File → New

Technology template → Netlist → Layout file
Layout screen after import of the Netlist
In LAYOUT Block:

- Establishment of design restrictions:
  - board outline
  - no. of layers
  - track widths
  - padstack assignments
  - route spacing

- Component placement

- Routing

- DRC and final operations

- Postprocessing: Gerber and NC Drill files, Printing, Reports
POST-PROCESSING

Options → Gerber Settings

Options → Post Process Settings
Proiect finalizat în Orcad Layout

Postprocesare Top layer
Postprocesare- Bottom layer

Postprocesare Masca de inscripționare - Silk Mask
<table>
<thead>
<tr>
<th>SYM</th>
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<th>TOL</th>
<th>QTY</th>
<th>NOTE</th>
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<td>8</td>
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<tr>
<td></td>
<td>0.120</td>
<td></td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>TOTAL</td>
<td></td>
<td></td>
<td>150</td>
<td></td>
</tr>
</tbody>
</table>

Postprocesare Drill Drawing
Postprocesare Solder Mask

Postprocesare- Assembly Drawing
Exemple de operații finale
Presentation of the thermal data acquisition system Politemp II

- The system POLITEMP II uses thermocouples and is primarily destined for temperature measurements of a reflow oven.

- It uses 8 measurement channels and is calibrated for K type thermocouple. For cold junction compensation an absolute temperature sensor is used (LM 35).

- Can be used in data acquisition mode, connected to a PC or "stand alone" as a portable "data logger”. In this last case the data are subsequently downloaded to a PC.
POLITEMP II

Echipament de masura destinat
managementului termic al modulelor electronice

Proiect de diploma al studentului:
Bogdan - Alexandru ROSU
Iunie 2004
Echipament de masura destinat managementului termic al modulelor electronice
Block Diagram of Politemp II Acquisition System
G = 1 + (50K/Rg)  
39.5μW/c + 500 = 19.73μW  
2.5/0.01975 = 126.58  
Rg = 50/126.58 = 398.145Ω
Schematic Page 2 of Politemp II
Top view of the main PCB assembly
Picture of the bottom side of the main PCB
Special Orcad techniques used in design:

- Intertool Communication (Cross Probing)
- Copper Pour
- Copy tracks
Cross Probing between Capture and Layout is very useful for complex projects, especially for component placement.
Power planes are required for better decoupling of digital circuits, shielding or are required by thermal reasons.

Usually the power planes are connected to ground.

In complex modules using mixed analog-digital processing, there exists more “grounds” that are connected together, usually at one point.

Orcad has the possibility to realize the so called “Split Power Planes”.

In our example there is a different situation: There is only one ground called “GND” and the planes are manually created.

The common point is the negative pole of the filter capacitor.
Obstacle 1- “Analog” Ground

Obstacle 2- “Digital” Ground

Obstacle 3- “Power” Ground

Bottom layer without Copper pour enabled- contour representation only
Bottom layer with Copper pour enabled
Copper Pour

The connection of pads to the plane is controlled by the line:

THERMAL_COPPER_POUR_VIAS=YES

from LAYOUT.INI file

Thermal Relief

No Thermal Relief, pads are “flooded” in surrounding copper
To create Copper Pour areas:

1. Create an obstacle (contour) of type “Copper pour”
   - Select Layer
   - Width
   - Clearance
   - Net Attachment

2. Activate the copper pouring from User Preferences menu
Copying Tracks

In some designs there are blocks (part) of circuit that are identical.

E.g. from our example the 8 processing channels for the thermocouples.

A good idea is to route one circuit and to copy the route pattern for the rest. This will save time and on the other hand a good similarity between the 8 channels is assured.

Many users claim the lack of ability to multiply the routing pattern.

Solution: Using of CAM programs and editing of Gerber files.

Drawback: No backannotation is possible and errors can appear.

Orcad version 10 comes with the concept of “Design Reuse”. The schematic must be initially prepared for that. Each reused block must be drawn in an hierarchical block and other special preparation are required for Netlist import. In the end, in Layout: Auto→Design Reuse.

Orcad version 9 has the Copy Tracks feature.
The tracks follow the same pattern.
To copy tracks:

1. Place the similar parts of the circuit at exactly the same relative distances. (How?)

2. Route the first “Master” pattern that will be copied.
To copy tracks (next):

3. Frame select the tracks using one of the routing tools and use CTRL+C or INSERT key to make a copy of the tracks. The tracks are moving together with the cursor.

4. Stop the cursor where the track segments fit and do “click”. The tracks are copied and the result is an identical track pattern. Connections corresponding to tracks must already exists. If the placement is different or connections are not present the operation fails.
NATIONAL STUDENT CONTEST
http://www.tie.ro
INTERCONNECTION TECHNOLOGIES IN ELECTRONICS (TIE)
Concursul TEHNICI DE INTERCONECTARE IN ELECTRONICA (TIE) este un concurs profesional studentesc ce are drept obiectiv proiectarea tehnologica asistata de calculator (CAE-CAD-CAM) a modulelor electronice.

http://www.tie.ro

Concursul reuneste studenti din mai multe centre universitare si este deschis tuturor studentilor pasionati de domeniu. Prin modul de organizare si corectarea publica a lucrariilor concursul isi propune sa promoveze spiritul de competitivitate si profesionalism in randul studentilor interesati de packaging-ul electronic.

La concurs au participat studenti, indiferent de facultate, care au cunoscut programe de proiectare asistată de calculator în domeniu, cu licenta. Pentru detalii suplimentare poate fi contactat directorul concursului, conf. dr. ing. Norocel Codreanu (norocel.codreanu@cetti.ro).
TEHNICI DE INTERCONECTARE ÎN ELECTRONICĂ

Concurs profesional studenţesc
Faza națională, Ediția a XVI-a
Suceava, 12-14 Aprilie 2007

Concursul vizează verificarea cunoștințelor concurenților în domeniul proiectării asistate de calculator a modulelor electronice.

Prin modul de organizare și corectarea publică a lucrărilor, concursul își propune să promoveze spiritul de competitivitate și profesionalism în rândul studenților interesăți de packaging-ul în electronică.

Participă studenți din centrele universitare:
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- BUCUREȘTI
- CLUJ-NAPOCA
- GALAȚI
- IAȘI
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