2. Modelling, simulation and design of interconnection

2.1 Introduction

Modelling and simulation methods and tools have long been used in the development of electronic microsystems to predict performance capabilities to ensure suitability to the given task. The goal of the analysis is to create a design that works at the specified performance on the first iteration. As the complexities of electronic microsystems grow, and as design cycle times shorten, more attention is focused on transforming modelling into a co-design activity used to optimize chip, package layout, and architecture for maximizing the performance at the low costs.

The goal of electrical modelling is to accurately analyze the entire microsystem, from source chip/package through the PCB and into the receiving chip chip/package. At higher frequencies, more structures throughout the system approach significant fractions of a wavelength with concomitant risks of coupling through electromagnetic interference (EMI). Use of transmission lines or waveguides is increasing, making timing analysis more critical and requiring that manufacturing variations such as dielectric thickness and trace widths be included. For 3-D packaging approaches such as stacked dice, stacked packages (Package On Package - POP) and interconnect technologies such as Through Silicon Via (TSVs), engineers must consider coupling to the above-die and below-die structures.

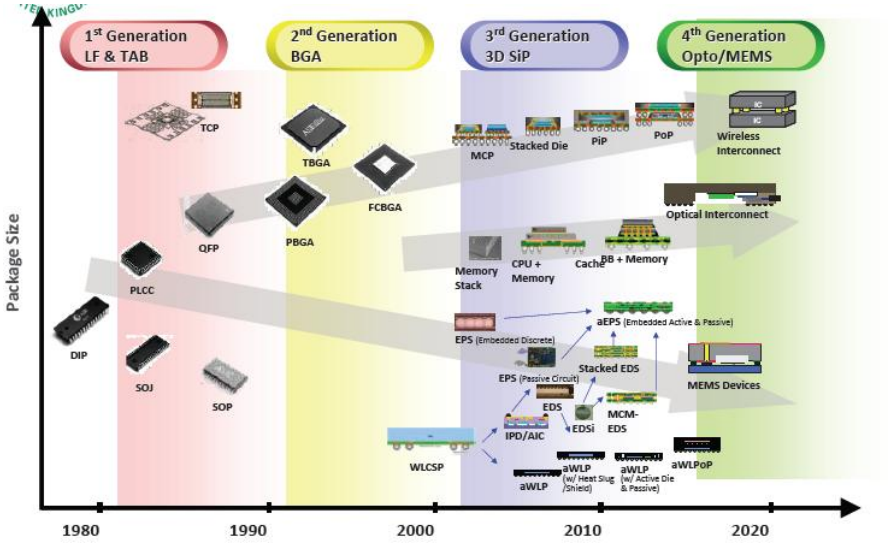


Fig. 2. 1 Structures, packages, and microsystems under investigations today and in the future

Electrical problems relate to both signal propagation in/between the chips/packages and to power distribution required to operate these transistors. The electrical parameters such as resistance, capacitance and inductance are always present and cause signal delays and signal distortions. Signal degradation is another problem that is due primarily to line resistance. Line resistance causes a voltage drop, thus increasing transition time. The power distribution problems stem from simultaneous switching of millions of transistors in a given circuit, resulting in drawing a big amount of current. This is referred to as "switching noise" (delta-I noise).

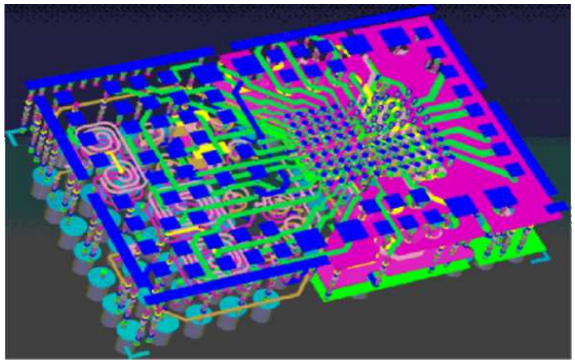


Fig. 2. 2 Example of a complex interconnection structure modelled for signal integrity (SI) & power integrity (PI) simulation and other advanced investigations (source: Mentor Graphics)

Since an electronic microsystem involves usually more than one IC, effective communication between one transistor on one IC and another transistor on another IC, all the way through system-level board with the required signal quality, is required. Signal communication, however, does not start until an appropriate power is supplied to each and every transistor. Power distribution, however, poses a whole set of challenges that include voltage drop as a result of long and high resistive wiring from the power supply to the transistor through all the levels of packaging. Signal distribution poses a different set of problems such as "cross-talk" between lines, as well as „distortion", „reflection" and „time skew". Electromagnetic radiation, as a result of all this radiated energy is another electrical challenge. In the figure 2. 3 a cross-section into a complex zone of a microsystem is depicted. In order to start from one point (one transistor) and to end to another point (another transistor) the signal must travel from the chip through its internal interconections, after this through balls/wire bonds to the package, after this through package balls/terminals, after this through PCB tracks, PTH vias, micro-vias placed onto/between various electrical layers and, finally, to reach the end point into another chip, back through balls/wire bonds of the end package and through the internal interconections of the end chip.

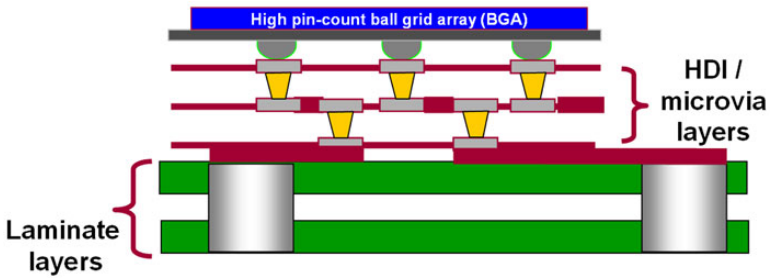


Fig. 2. 3 Cross-section into a complex zone of a microsystem

One of the new numerical methods and tools that are currently emerging is based on molecular modelling. It is well known and used in chemistry, biology, medicine, biotechnology, pharmacy and physics. Molecular modelling and simulation enables to control structure and properties of the materials in the nano-scale. Molecular modelling also ensures control of processes and prediction possibility. A possible area of application of molecular modelling is also microelectronic packaging, for solving problems that occur in surface phenomena, thin films, viscoelasticity or mechanical and thermal properties of novel materials and compounds. Numerical modelling techniques and tools can be divided according to the relevant time and length scale and domain (figure 2. 4).

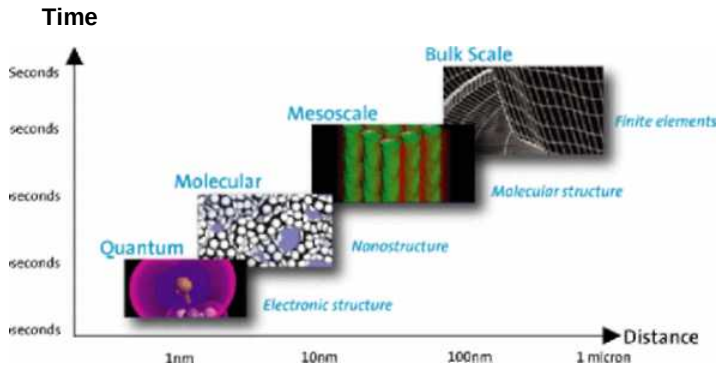


Fig. 2. 4 Time and length scale problem in numerical modelling (source: accelrys.com)

Molecular modelling is based on the following paradigm and phenomena: force field, first principles quantum mechanics calculation, Van der Waals energy, Coulomb energy, etc. Taking into account the above, it can be summarized that molecular modelling seems to have a number of benefits in reference to microelectronics of which the most important ones are: field gradient problem, second order phenomena, multi-physics, stochastic behavior, discrete description. Additionally, it should be underlined that molecular modelling is especially suitable for computational material and engineering, which allows for:

- prediction of novel structural and functional materials, e.g., nanomaterials;
- optimization of complex materials/design solutions;
- simulation of materials synthesis, processing, microstructures and properties;
- development of history-dependent and of scale-bridging multi-scale simulation concepts;
- integration of electronic and atomic level as well as continuum;
- studying phenomena that are not easily accessible by experiment;
- solving cost and time constraints for materials development and application.

At the package level of microsystems, High Density Interconnect (HDI) techniques and technologies represent a way to condense electronic circuits for ruggedness, radiation hardening, and high performance. HDI minimizes the size and weight of electronic products while maximizing their performances. HDI circuits offer new solutions to signal integrity (SI) and electromagnetic compatibility (EMC) concerns, concerns which are expected to grow more and more as rise/fall times continue to drop.

High Density Packaging (HDP) or High Density Interconnects (HDI) are defined as advanced interconnection structures with a higher wiring density per unit area than conventional printed circuit boards (PCB) and special elements, as microvias (see figure 2. 3). Table 2. 1 offers a short characterization of HDI parameters.

Parameter	Value
W	<75 µm (3 mil)
S	<75 µm (3 mil)
Via hole	<150 µm (6 mil)
Via capture pad	<400 µm (16 mil)
Pad density	>20 pads/cm^2

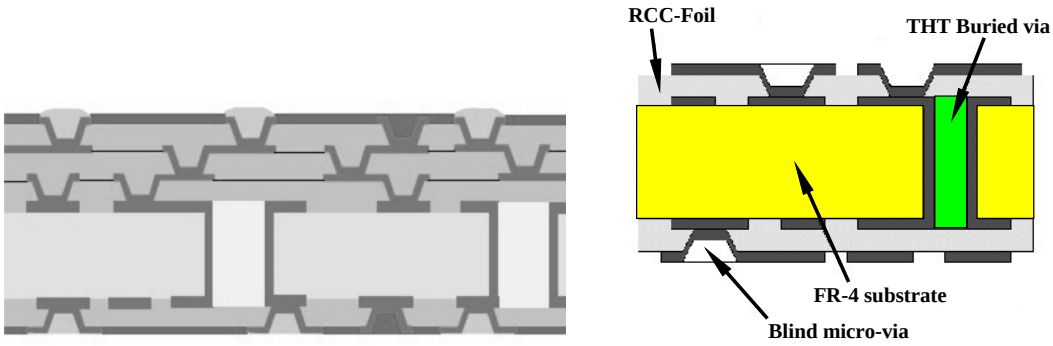
Tab. 2. 1 Parameters of HDI

HDI is used to reduce size and weight, as well as to enhance electrical performance. Similar terms with HDI are "microvia boards", "build-up boards" and "sequential build-up (SBU)". Companies involved in HDI now have to deal with various constraints in order to meet

electromagnetic compatibility (EMC) requirements. Due to continuous miniaturization, higher clock frequencies, faster edge times (rise and fall) and more functionalities, the electromagnetic problems are causing more and more troubles in several application areas, such as automotive, multimedia, telecommunication, and computing. Because PCB manufacturers have developed new materials and technological solutions, indispensable at this moment is to perform a deep virtual characterization of structures directly related to HDI. This paragraph presents investigations and results focused on the main areas of SI and EMC, as noise at PCB level (reflections, and crosstalk), electromagnetic interference (EMI) and on-board interconnection delay. Various HDI-PCB items and structures were evaluated using the MoM full-wave electromagnetic simulation method. After modelling and simulation a link to classical circuit simulators was created by extracting RLCG elements and various parameters, which are directly related to the total current along the HDI structures.

Additionally, because today the vias density is also an important electrical issue, vias between signal tracks or power/ground stubs from signal layers to reference planes were studied. The more vias on a board, the more discontinuities into PCB/MCM passive interconnection structure are placed. In these conditions, one shall be presented the effect of different via types on the characteristics of the high speed/high frequency interconnection lines.

Based on such virtual investigations, high-quality designs will minimize the electromagnetic interference in HDI, offering an appropriate methodology for future projects. Therefore methods and electromagnetic software tools for an improved design taking into account the boundary conditions and appropriate integration into design processes is a major challenge for the global electronics industry today.



a) b)

Fig. 2. 5 HDI structures: a) 6 layers b) 4 layers

Although the technology would seem to be prohibitively expensive, it can actually lower costs due to a reduction in (traditional PCB) laminate layers and smaller boards (e.g. more boards per panel). To facilitate increased on-chip functionality, additional passive devices (e.g. terminating resistors and decoupling capacitors) are required. By some estimates, passive components constitute 70-80% of the total part count, and this percentage continues to grow as passive-to-active ratios grow. While the active components are being packaged into larger ball grid arrays (BGAs), the ideal surface placement space for discrete passive components becomes more difficult to obtain. Currently, using surface mount device passives mounted on the top and bottom of a PCB takes up a lot of space and since some discretes must be placed away from the FPGA they serve, this can have a negative effect on system performance. By embedding these passives on the inner layers of the PCB, designers can significantly reduce the size of the PCB (see figure 2. 6) and optimize the performance.

Addressing the challenges of embedded passives leads to some important benefits (besides size). Using embedded passive components allows for higher frequency (faster) PCBs. The linearity of signals through embedded integral passive components reduces inductance of “core to surface, return to core” signal paths. Along with lower inductance, embedded integral passive components can lower power system impedance and radiated emissions – improving the overall electrical performance of a PCB. Using embedded components can also lead to reduced microsystem costs. This includes the overall system costs that are reduced by eliminating SMDs (components, assembly) and board area. In addition, more boards per panel can be obtained, a smaller bill of materials (BOM) is necessary and there is less rework time and cost.

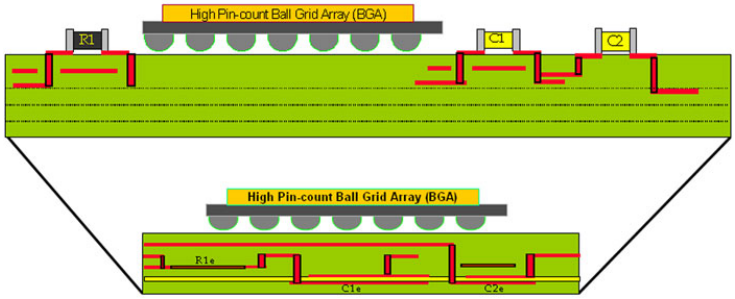


Fig. 2. 6 Minimizing a classical PCB with discrete passive SMDs to the stage of advanced PCB with embedded passives into the substrate

Note that ultra-small product form factors have also driven the need for embedded discrete active components. While additional surface space is made available for other active components, embedded discrete active components are not packaged, leading to smaller footprints for the active component.

2.2 Meshing and cells

For solving the problem, the HDI structure under evaluation is decomposed basically into a substrate layer stack and various conductive patterns, which are meshed using elementary triangular and rectangular cells (figure 2. 7). Maxwell’s equations are translated into integral equations by imposing the boundary conditions on the planar structures. The primary formulation of the IE3D (the software system used) is an integral equation obtained through the use of Green functions.

Planar electromagnetic simulators, also referred to as 2.5D EM simulators, rely on the method of moments (MoM) to discretize and solve Maxwell's equations for planar circuits embedded in a multilayered environment. These simulators traditionally are being used to model the distributed coupling and radiation effects of microwave integrated circuit and planar antenna applications. The state-of-the-art planar electromagnetic simulator uses a mesh to discretize the currents on the planar structures. The current distribution is modeled with the so-called rooftop functions allowing for a piecewise linear current distribution. The corresponding charge distribution is piecewise constant and satisfies the local current continuity relation. This is an important property for the rooftop basis functions. At microwave and millimeter wave frequencies, the size and number of cells in the mesh is mainly determined by the electrical wavelength of the signals guided by the planar structure. Typically, at least 10 linear subdivisions per wavelength are needed to obtain accurate results.

Due to the accurate modelling of the surface current distributions, planar electromagnetic simulators allow to produce accurate electrical models for arbitrary power/ground and signal trace configurations up to the higher RF and microwave frequencies. These models follow directly from the physical interpretation of the electromagnetic interaction matrix equation in terms of an equivalent RLC network. Using only rectangular and triangular cells strongly limits the ability of the mesh maker to create efficient meshes with a low number of high quality cells. As a result, the required computer time and memory resources can be extremely high, which makes the planar electromagnetic simulators less efficient for simulating complex interconnection structures.

At the beginning, it is necessary to offer an overview of the method of moments technique behind the simulator and discuss the derivation of an equivalent RLC network model. This allows to give the MoM interaction matrix equation a physical interpretation by constructing an RLCG equivalent network model (figure 2. 8). It has a capacitor to the ground representing the electric self coupling of the associated charge basis function. All nodes are connected with branches which carry the current flowing through the edges of the cells. Each branch has in inductor representing the magnetic self coupling of the associated current basis function and a resistor representing the conductor loss due to the current basis function. Additionally, losses in the dielectric are presented in the equivalent model.

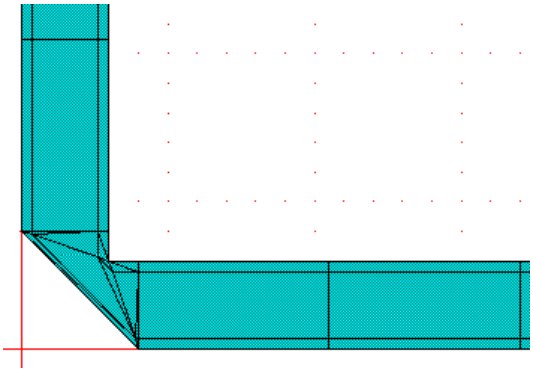


Fig. 2. 7 Conductive pattern (interconnection structure) and associated cells

The surface currents on the planar structure are modeled with basis functions defined over cells in the mesh. The boundary conditions are imposed by applying the Galerkin method. For obtaining the final results, a matrix equation (formula 2. 1) is generated.

$$\text{For i= 1…N } \sum_{j=1}^{N} Z_{i,j} I_j = V_i \text{ or [Z].[I]=[V]} \qquad (2.\ 1)$$

where impedances and voltages are:

$$Z_{i,j} = \iint_S B_i(r) \cdot dS \cdot \iint_S \overline{\overline{G}}(r,r') \cdot B_j(r) \cdot dS' \qquad (2.\ 2)$$

$$V_i = \iint_S B_i(r) \cdot E(r) \cdot dS \qquad (2.\ 3)$$

Each impedance element (Zi,j) represents the electromagnetic interaction between two basis functions Bi(r) and Bj(r) placed in the substrate layer stack. Each element Vi in the excitation vector represents the discretized contribution of the sources applied at the ports of the HDI structure. The solution of the matrix equation yields the expansion coefficients for the unknown

surface currents (formula 2. 4), which contribute to the electromagnetic field in the interconnection structure by means of the Green dyadic function of the substrate layer stack.

$$J(r) = \sum_{j=1}^{N} I_j B_j(r) \tag{2. 4}$$

The Green function is decomposed (see the mixed potential integral equation/MPIE formulation) into a sum of contributions from the vector potential A(r), the scalar potential V(r) and a term related to DC and AC (skin effect) losses.

$$\overline{\overline{G}}(r,r') = j\omega G^A(r,r')\overline{\overline{I}} - \frac{1}{j\omega}\nabla[G^V(r,r')\nabla'] + Z_s\delta(r-r')\overline{\overline{I}} \tag{2. 5}$$

The scalar potential originates from the dynamic surface charge distribution derived from the surface currents, being related to the vector potential through the Lorentz gauge. The surface impedance Zs depends on the conductivity and thickness of the conductive (metallic) structure and models the frequency dependent skin effect loss. Substituting the expression (2. 5) for the Green function into the expression of impedance elements Zi,j (formula 2. 2), yields the following form:

$$Z_{i,j} = R_{i,j} + j\omega L_{i,j} + \frac{1}{j\omega C_{i,j}} \tag{2. 6}$$

with:

$$Z_{ij}^L = j\omega L_{ij}(\omega) = \iint_{S_i} dS \iint_{S_j} G_m(\omega, r-r')B_i(r)\cdot B_j(r')\cdot dS'$$

$$Z_{ij}^C = \frac{1}{j\omega C_{ij}(\omega)} = \iint_{S_i} dS \iint_{S_j} G_e(\omega, r-r')\nabla\cdot B_i(r)\nabla\cdot B_j(r')\cdot dS'$$

$$Z_{ij}^R = R_{ij}(\omega) = Z_s(\omega)\iint_{S_i} dS \iint_{S_j} \delta(r-r')B_i(r)\cdot B_j(r')\cdot dS'$$

This allows to give the MoM matrix presented in the first formula (2. 1) a physical interpretation by generating an RLCG equivalent circuit (figure 2. 3).

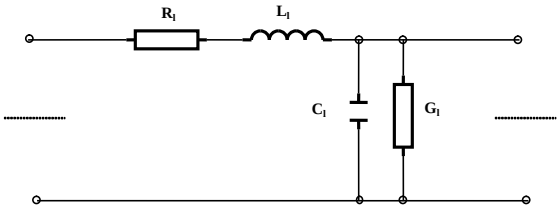


Fig. 2. 8 RLCG equivalent circuit of an interconnection

The nodes correspond to the cells in the mesh and hold the cell charges. As presented above, each cell corresponds to a capacitor to the ground representing the electric self coupling of the associated charge basis function and all nodes are connected with branches which carry the current flowing through the edges of the cells (figure 2. 8). In the figure 2. 9 only the capacitive and inductive elements are depicted.

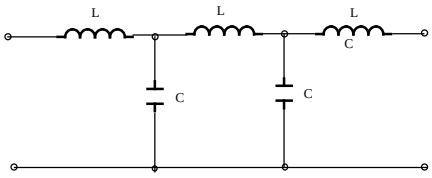


Fig. 2. 9 Segment with capacitive and inductive nodes and the LC equivalent circuit

The MoM matrix equation (2. 1) follows from applying Kirchoff voltage laws in the equivalent circuit. The inductor branch currents in the circuit follow from the solution of this matrix equation and represent the coefficients of the basis functions in the expansion of the surface currents. The use of basis functions allows to give a physical interpretation to the currents in the network, that is, the circuit currents correspond to the total normal current flowing across the edges in the mesh:

$$I_j = \int_{edge[j]} J(r) \cdot u_n \cdot ds \tag{2. 7}$$

The physical interpretation for the voltages in the circuit follows from power conservation considerations. The complex power delivered to the surface current J(r) = IjBj(r) is given by:

$$P_j = \frac{1}{2} \iint_S E(r) \cdot J^*(r) \cdot dS = \frac{1}{2} [\iint_S E(r) \cdot B_j(r)] \cdot I_j^* \cdot dS \tag{2. 8}$$

Based on a full-wave approach, in IE3D the magnetic and electric Green functions follow from Maxwell electromagnetic equations which include all coupling, radiation and dispersion effects in the substrate. These Green functions and as a result, also the inductors and capacitors in the RLC equivalent circuit, are complex and frequency dependent (formulas from below (2. 9) present the case of free space):

$$G_m(\omega, r - r') = \frac{j\omega\mu_0}{4\Pi|r - r'|} e^{-jk_0|r-r'|}$$

$$G_e(\omega, r - r') = \frac{1}{j\omega\varepsilon_0 4\Pi|r - r'|} e^{-jk_0|r-r'|} \tag{2. 9}$$

where: $k_0 = \omega\sqrt{\varepsilon_0\mu_0}$

The network elements of the equivalent RLC network can be calculated using either a fullwave approach or a quasi-static approach. These two approaches differ in the type of Green's functions used to calculate the L's and C's. Due to the use of the electrostatic and magnetostatic Green's functions, the resulting L's and C's are real, frequency independent and do not include the high frequency wave effects (radiation). For low frequencies or electrically small distances, the static terms dominate and the quasi-static approach will yield similar results as compared to the fullwave approach. As the frequency increases and the electrical length of the circuits becomes significant, the quasi-static results will gradually deviate from the fullwave results.

Uniform and non-uniform grids for electromagnetic simulation

For general purpose electromagnetic simulators, a meshed structure (with triangular, rectangular or polygonal elements) is used. The efficiency of the meshing can be greatly enhanced by removing the restriction imposed by the use of rectangular and triangular cells in the mesh. This is realised by adopting the concept of mesh reduction. Starting from an initial mesh of rectangular and triangular cells, a new mesh is constructed by merging two or more adjacent

cells. This results in a "reduced" mesh with a lower number of "generalized" polygonal shaped cells. The mesh reduction step can be repeated in consecutive steps up to the highest level, in which each disconnected metallization pattern is represented by only one "generalized" cell in the mesh. With each level in the reduced mesh, an electromagnetic equivalent network can be constructed by applying the method of moments discretization. This comprises a generalization of the basis functions used to model the surface currents in the polygonal shaped cells. In the resulting equivalent network, the capacitors model the charges built up in the generalized cells and the inductors model the current flowing from one generalized cell to another. It is clear that the electromagnetic equivalent circuit corresponding to the lower reduction levels have fewer elements and can be solved much faster, leading to a reduced equivalent EM-based network model. Mesh reduction provides a way to overcome the limitations of traditional method of moment meshes that only use rectangular and triangular cells.

An important problem is whether the mesh has to be uniform or non-uniform. Uniform mesh is required for those simulators using the FFT to calculate the double surface integrals (formula 2. 8). For uniform grid based simulators, the layout is divided into a uniform grid. Then, the designer creates the circuit based upon the existing grid points. The process is basically a procedure of fitting the particular circuit into the uniform grid (figure 2. 10). If your circuit can not be fitted into the uniform grid, there are two choices. One is to cut the portion can not be fitted and the other is to make the uniform grid finer (to increase the number of cells in the same area) in order to get a better approximation. In case of MoM, making the grid twice as fine means that to quadrupling the number of cells, leading furthermore to a processing time much longer (the solution is obtained at least 16 times slower, which can create problems in case of complex structures).

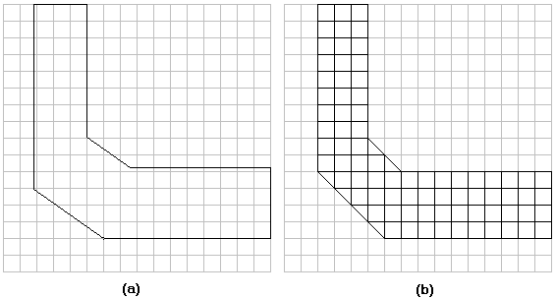


Fig. 2. 10 Circuit placed in an uniform grid

Uniform grid imposes a biggest accuracy and efficiency limitation on uniform grid based electromagnetic simulators but creates large number of cells. For example, figure 2. 10a presents a microstrip bend structure with the layout placed in a uniform grid but the bend is not matched with the grid. To solve this problem, the bend is changed in order to fit into a uniform grid (figure 2. 10b). The cells inside the fitted structure are the cells used in the actual calculation (83 cells).

To improve the simulation speed, IE3D is based on a triangular and rectangular mixed meshing scheme and apply the non-uniform grid basis function on it. A non-uniform grid based simulator approaches a problem in a better way. The designer creates the circuit inside a layout editor, having no concerns about the number and shape of cells. Then, the simulator tries to fit a non-uniform triangular and rectangular mesh into the circuit. The main advantage is that the simulator tries to create a non-uniform mesh to fit the circuit instead of trying to fit the circuit into a pre-defined mesh. Figure 2. 11 shows the same microstrip bend structure with two particular discretization schemes and, by comparison between figures 2. 10 and 2. 11, the non-

uniform grid meshing schemes are more flexible, efficient and accurate than the uniform meshing scheme. The circuit, based on the non-uniform grid and non-uniform cells, can approximate more accurate the real planar interconnection structure, especially in case of HDI (where dimensions are smaller than in classical PCB) and microsystems structures because in the zones of highest interest (corners, vias, step in width, etc.) the number of cells is much higher and very good fitted with the specific geometry (figure 2. 11).

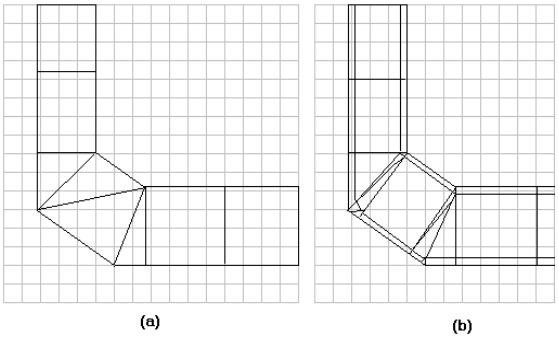


Fig. 2. 11 Circuit placed in a non-uniform grid

Non-uniform grid is flexible, efficient and also accurate. Figure 2. 11a presents a coarse non-uniform meshing (with 8 cells) of the structure from figure 2. 10a. As can be quickly observed, no approximation is made in the shape of the planar circuit. Total 8 cells are created. Figure 2. 11b presents small edge cells which are automatically created on the edge of the HDI track in order to enhance accuracy (29 cells). The small cells along edges of the structure are used to model the edge singularity of the current distribution (see figure 2. 12). Even a circuit based on an uniform grid creates more freedoms in the calculation, it does not mean that it is more accuracy than a non-uniform grid based simulator due to the fact that the uniform grid based simulators do not use all those cells in the right place even they have more cells. For current density simulation in the transverse direction, 1 - 5 cells are used (figure 2. 12), offering a sufficient good accuracy for current density at the edges of the planar circuit. MoM is accurate in predicting the total current on the transverse direction even using 1 to 5 cells in the transverse direction. For fast simulation, IE3D uses 1 cell in the transverse direction and still gets reasonable accuracy. To get high accuracy an increased number of cells along the edge of the strip can offer a solution.

For HDI layout design, especially in case of HDI development and optimization based on electromagnetic modelling and simulation, the most important parameters are Z, Y, and S. These parameters are directly related to the total current on the transverse direction at a port. So, the parameter a circuit designer really cares about is the total current which is the integral of current density instead of the current density itself. In order to manage better EMI (Electro-Magnetic Interference) issues, where various parasitic antennas existing into a HDI layout can create large problems, a designer is interested in the radiation pattern which is also a weighted integral of current density.

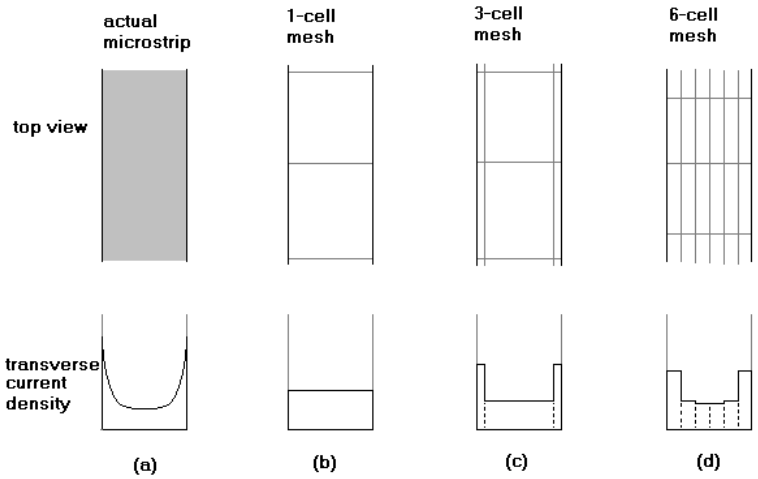


Fig. 2. 12 Current density modelling (1 - 5 cells) in the transverse direction

Mesh reduction

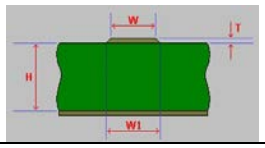
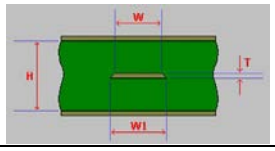
The planar electromagnetic investigation methods provide an easy way to construct an equivalent network of mutually coupled inductors and capacitors. The number of self and mutual coupling elements in this network is determined by the number of cells in the mesh. The complexity of the equivalent network (or the efficiency of electromagnetic solution process) depends strongly on the density and quality of the mesh. Basically, the size and the number of rectangular and triangular cells are mainly determined by the electrical wavelength of the signals travelling into the planar structure. When simulating analog/digital, high frequency interconnections and packaging structures at the lower radio frequencies, the geometrical complexity of the metallization patterns leads to a much higher number of cells than needed by the mesh density wavelength criterium. The rectangular and triangular cells limit greatly the possibility to generate efficient meshes (with low number of complex cells). In the case of geometrically complex but electrically small structures, the meshes contain a very (and, even, too...) large number of rectangular and triangular cells, leading to the conclusion that planar electromagnetic simulators are less attractable for investigating large high frequency boards and packaging structures.

The efficiency of the discretization is strongly enhanced when it is possible to use more than only rectangular and triangular cells. This is realised by adopting the concept of mesh reduction. Starting from an initial mesh of rectangular and triangular cells, a reduced mesh is constructed by merging two or more adjacent cells. This results in a lower-resolution mesh with a lower number of more complex polygonal cells. The mesh reduction step can be repeated up to the highest level, in which each disconnected metallization pattern is representing by only one complex cell in the mesh. With each reduced level, an electromagnetic equivalent circuit can be build. In this equivalent circuit, the capacitors model the charges build up in the complex cells and the inductors model the current flowing from one complex cell to another. Starting from the solution of the lowest reduced level allows to build a series of simulation results with increased accuracy. The calculation of inductive and capacitive interactions in the complex mesh relies on the definition of generalized basis functions for polygonal shaped cells. These polygonal shaped functions are used as the basis functions in the method of moments discretization on the generalized mesh. They are the natural extension of the classical rectangular and triangular rooftop functions. Mesh reduction can provide a way to overcome the limitations of traditional method of moment meshes which use only rectangular and triangular cells. The use of mesh reduction allows to eliminate low-quality slivery cells from the mesh, to generate meshes for

geomatrically complex structures with fewer cells, to reduce the computer memory required to store the interaction matrix, to reduce the computer time needed to solve the interaction matrix, and to generate multiple levels of meshes with different resolutions

2.3 Layer stack-up and thickness

The graphical editor of the electromagnetic simulator uses a two layers system for planar interconnection structures description: dielectric substrate layers and metallic layers. The dielectric layer system is defined in the "Substrate" in "Param" menu. By default, the no.0 dielectrics is always at z = 0. The default no.0 dielectrics is always the ground plane. Mathematically, a finite thick or infinite thick ground plane yields the same result when they are large in the horizontal directions. The metallic layer system is created based on the dielectric system. Table 2. 2 shows two examples of the layers stack-up in case of microstrip and stripline geometries.

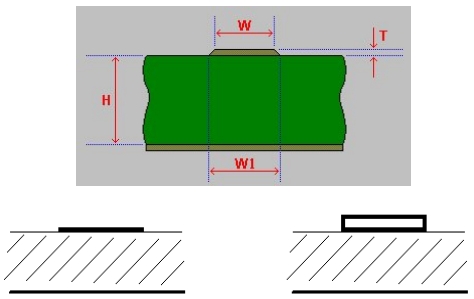
Cases	Layers stack-up	Parameters
Microstrip H(thickness)= 40mil, ε_r= 4.7 loss tangent = 0.02	Air Substrate ε_r = 4.7 GND Plane 	No.0, Ztop=0, Epsr=1, Sigma=(5.8e7) S/m No.1, Ztop=40, Epsr=1,Sigma=(0,0) S/m
Stripline Metallic track is at the middle. H(thickness)= 60mil ε_r =4.7 loss tangent = 0.02	GND Plane Substrate ε_r = 4.7 Substrate ε_r = 4.7 GND Plane 	No.0, Ztop=0, Epsr=1, Sigma=(5.8e7) S/m No.1, Ztop=60, Epsr=4.7, Sigma=(0,0) No.2, Ztop= 0e+15, Sigma=(5.8e7) S/m

Tab. 2. 2 The layers stack-up for EM simulation

Regarding the thickness of interconnection metallic structures, there are two methods to model it. The default and simplest way is to use infinitely thin strip to model the structure. In addition, IE3D uses analytical formula for the surface impedance (Zs) in order to model the loss effect of the strip. The skin effect is included in the analytical formula for the Zs. The infinitely thin strip model is good when the following condition is satisfied: track width (Wtrack) is much bigger than the track thickness (t).

$$W_{track} >> t \qquad (2.\ 10)$$

The second method is a more accurate model for thick tracks. Instead of approximating the tracks as infinitely thin tracks, the software package model the current on the 4 sides of the track. The obtained model yields better L and C calculation. The main problem in this case is regarding losses.



a. b.

Fig. 2. 13 Modelling of interconnections thickness

The „a" case presents the cross-section of the infinitely thin track model (microstrip geometry), where the current is assumed on the one single track only. The „b" case presents the cross-section of the finite thick strip model where the current is assumed on the 4 sides of the strips. The track information will be used in finding the Zs for loss calculation but it is important to underline that the surface impedance modelling using MoM is always an approximation.

2.4 Practical modelling and simulation of microsystems interconnection structures/elements

In order to perform the full-wave MoM electromagnetic simulation, a 2.5D modelling was used to create the microsystems structures and elements under investigation. Figures 2. 14 and 2. 15 present a full IE3D investigation flow, containing also a FDTD package, and a part of a MCM-L-BGA package/module, which was the structure under evaluation. The MoM electromagnetic simulation was focused on three elements, as presented in the figure 2. 15: track, wire bond, and via. The elements are physically connected and form finally a transmission line for the signals travelling in the microsystem package/module. The deviding of the whole structure in elementary objects was necessary to be performed due to hardware limitations and processing time optimization.

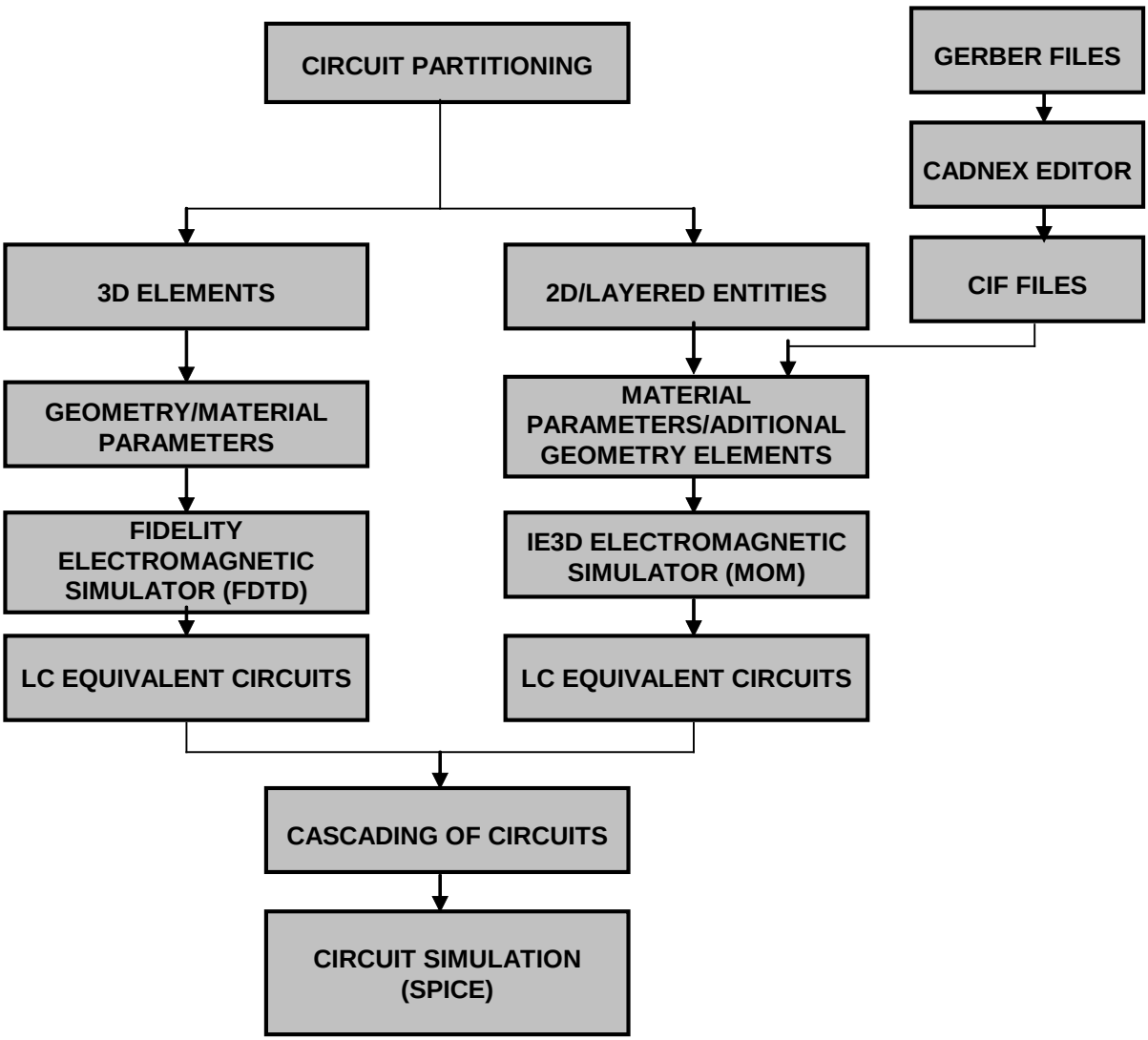
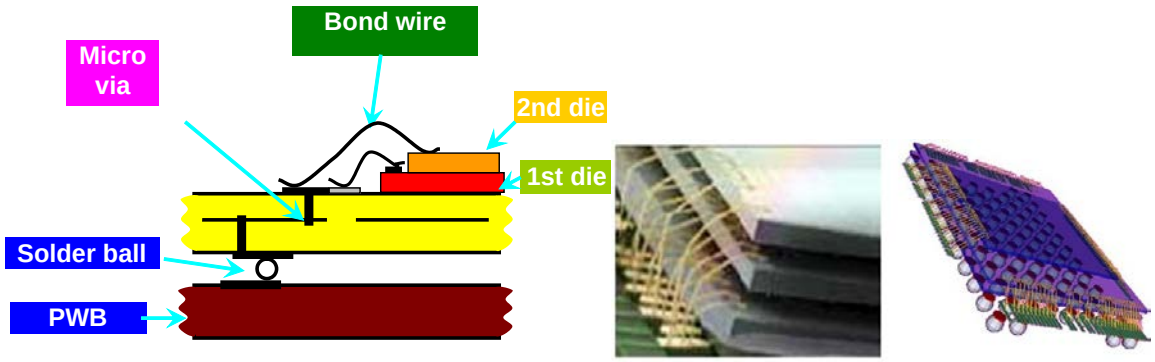
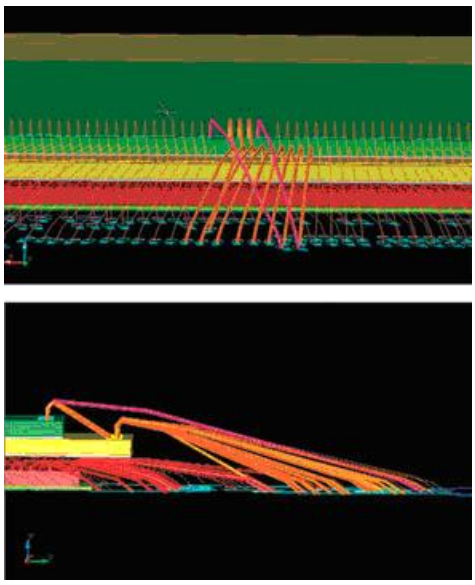


Fig. 2. 14 Full-wave electromagnetic investigation flow

Each element was transformed into a layered finite element structure which was investigated in the frequency range, at different frequencies and with different number of cells, followed by the electrical circuit simulation.



a. b.



c.

Fig. 2. 15 a) Elements and objects for simulation; b) Zoom of a complex stacked dice (chips); c) Modelling multiple wire bonds in the case of a complex stacked dice

In figure 2. 16 3D views of the investigated elements are presented. The via has the copper pad of 12 mil and the drill diameter of 6 mil. The track segment is of 1000 mils long and of 3 mil in width. The bonding wire is non-symmetric, having the wires for bonding of 1 mil (Gold) and 100 mil long. The pads sizes have 8×8 mils on PCB and 2×2/4×4 mil on chip/BGA.

Fig. 2. 16 HDI elements for simulation (track, wire bond, and via)

The electromagnetic simulation has offered a large number of data, some of them (for the wire bond) being presented below. The simulation parameters are: Accuracy Enhancement = 2, 3D Accuracy Enhancement = 2, Gridding Freq = 20 GHz, Automatic Edge Cell with Width = 0.2 mil, Meshing optimization enabled, Matrix Solution = 2, # GHZ Z MA R 50, Nport = 2, i=1 extension for MMIC, cell=3, i=2 extension for MMIC, cell=3.

Simulation frequency [MHz]	Cells/Unknown	Matrix Solver	Time [s]
10	132/217	SMS (50 %)	184
50	132/217	SMS (50 %)	130
100	132/217	SMS (50 %)	120
500	132/217	SMS (50 %)	99
1000	132/217	SMS (50 %)	85

Tab. 2. 3 Simulation data for the wire bond

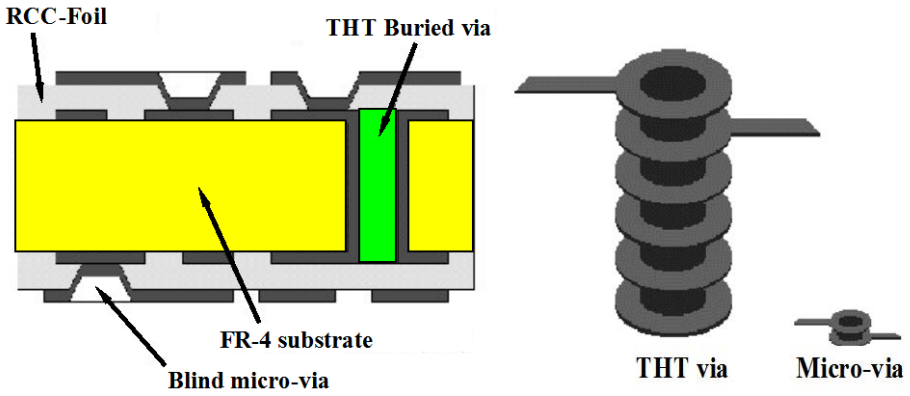
S parameters and LC equivalent circuits at frequencies in the range 0.01 ÷ 1 GHz were obtained. The results at three frequencies are in table 2. 4 shown. Having all LC parameters for the three

elements, the whole equivalent circuit for the structure can be easily drawn by connecting the three two-port networks.

Parameters Frequency [MHz] ↓	L[nH]	C[pF]
100	4.46	0.044
500	4.62	0.045
1000	4.82	0.047

Tab. 2. 4 LC Spice lumped model of the wire bond

3D average current densities of the simulated structures, near field and far field displays and all the parameters obtained after simulation are available for future research and studies. The resulting S-parameter data is back-annotated to the schematic design setup for a transient analysis. The interconnection structure is meshed at 5 GHz with a mesh density of 20 cells per wavelength. The original mesh was created with only rectangles and triangles. The geometrical complexity of the interconnection patterns implies a lot of redundant elements in the mesh, which are removed by applying the mesh reduction technology disscussed the previous paragraph. The resulting reduced mesh gives a reduced interaction matrix size of 1354. This results in a more than 10-fold improvement in memory usage and a more than 20-fold speed improvement for the electromagnetical simulation of the structure. The use of polygonal cells enhances the flexibility of the meshing and reduces the number of cells needed to discretize a given complex geometrical patterns, without loss of accuracy.

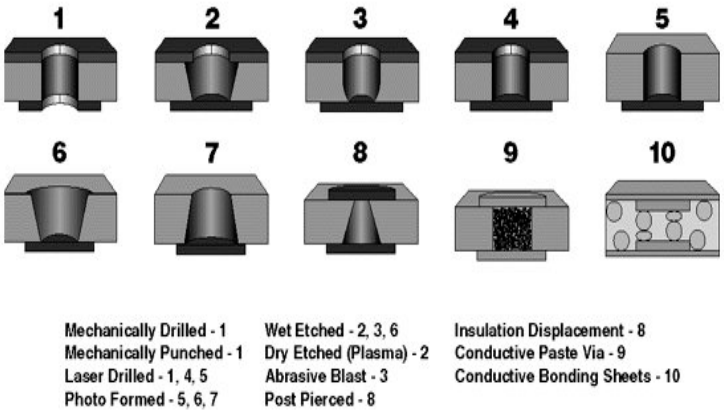


Courtesy of IPC; source: IPC webpage

Fig. 2. 17 Conventional through-hole via vs. microvia (not to scale)

In the case of via modelling and simulation, in figure 2. 17 a geometrical comparison between the dimensions of conventional vias and microvias is presented.

It is interesting to mention that today minimum values for them are 8…10 mils hole/20…25 mils via pad for conventional (THT) vias and 1…5 mils hole/8…12 mils via pad for microvias. Figure 2 offers information on different types, shapes and geometries of electrical vias existing in electronic products.



Courtesy of IPC; source: IPC webpage

Fig. 2. 18 Vias generated by different technologies

Shortly, a few techniques for vias manufacturing are available: mechanical (punching and drilling), laser (CO2, YAG and excimer lasers), photochemical (liquid or dry film resists) and etchings (wet or dry etching).

As it is well known, via represents a discontinuity with an inherent capacitive effect which cause a step-function change in the characteristic impedance of the signal line. The accumulation of excess charge in the spatial zone of via is realized both due to the corners and to the "padstack" (generated with two or more elements, see figure 1). The effect is larger increasing the frequency, the perturbing phenomena being considered important over 2...3 GHz. For analysis, modelling and simulation of vias and microvias it is necessary to start the discussion from the comparison between the hole diameter of via ("d") and the height of via (the distance, "h" between the two signal layers connected through this entity, figure 2. 19).

1. If **h >> d** via can be equated with a conductive barrel placed between "i" and "j" layers and the discontinuity will appear as a reunion of two corner discontinuities.
2. If **h ≅ d** or **h < d** the approximation from above is no longer valid and via barrel and via capture pads must be taken into account.

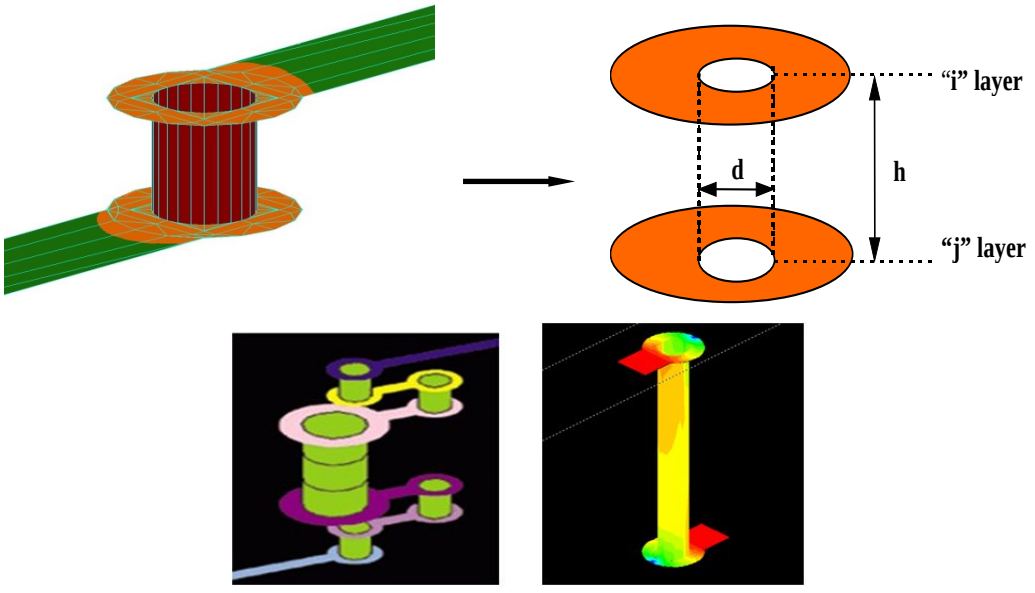


Fig. 2. 19 Geometrical sizes for vias evaluation ("d" and "h") and 3D views of various vias

Via is evaluated through the generation of 2.5D finite elements models based on IE3D method of moments (MOM) planar electromagnetic simulator. During the electromagnetic simulation process S-, Y-, Z- parameters of different types of via were calculated, and values of passive circuit elements (Spice lumped RLCG model) were obtained. In the first part the modelling and simulation of conventional mechanically drilled through holes were performed. For a proper management of hardware resources and for minimizing the CPU simulation time, the cylinder of via and the capture pads were created based on quadrilateral strips and octagons.

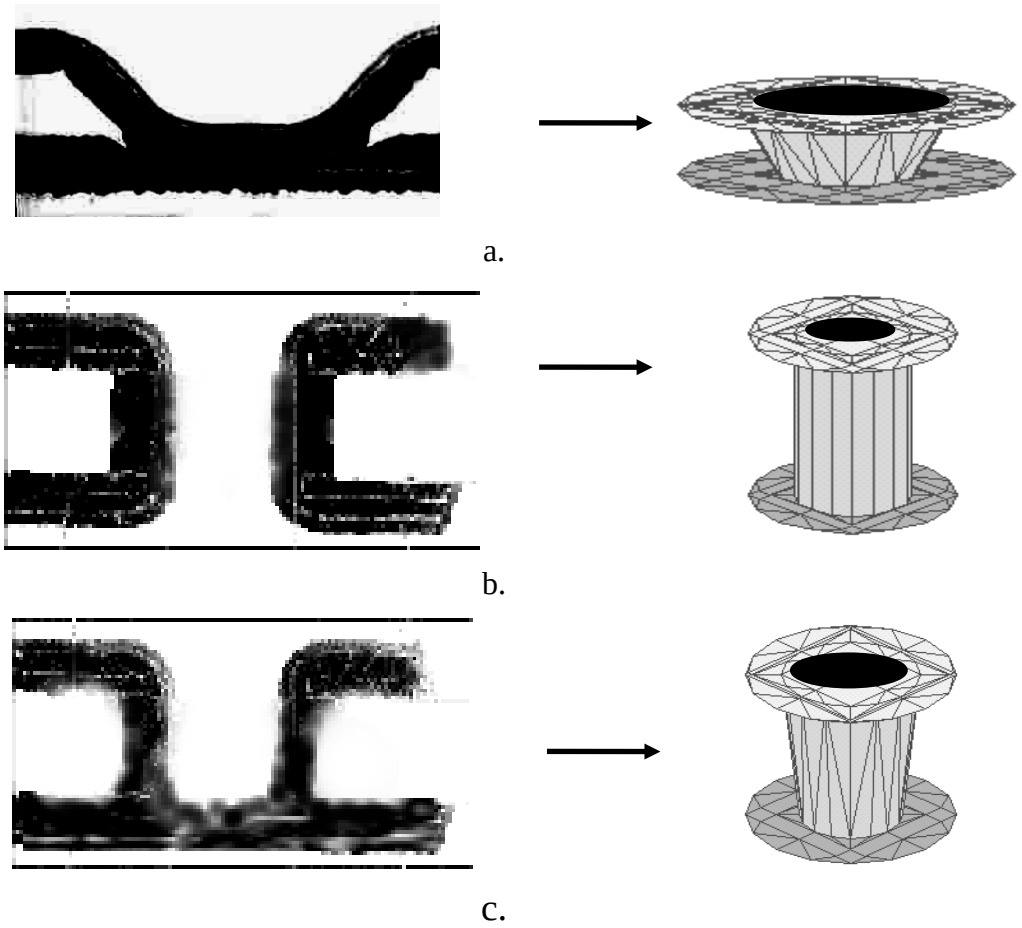
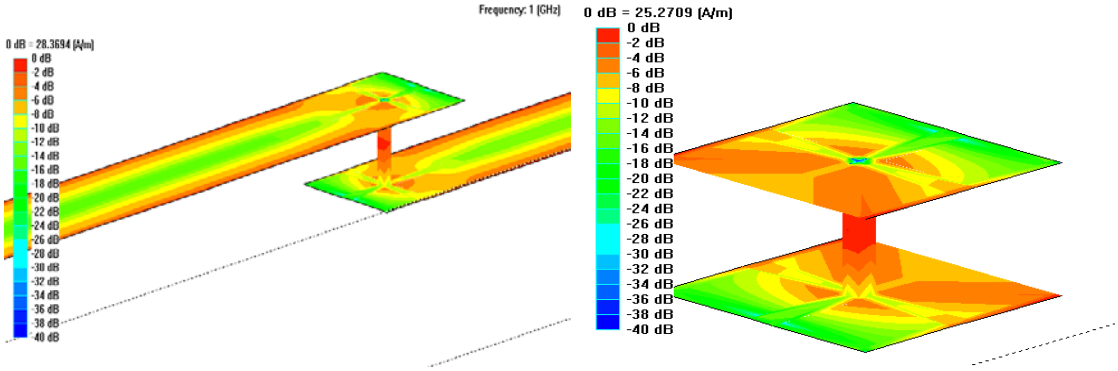


Fig. 2. 20 Correspondence between real vias and finite elements models (not to scale)
a) plasma ablation via; b) mechanically drilled via; c) laser ablation via

An advantage of the IE3D-MOM simulation is that the field and current distributions from a simulated structure are accessible for circuit/RF/microwave specialists for ulterior analysis. The via hole diameters of mechanical vias were (mils): 12, 16, 20, 24, 28, 32, 40, 80. Signal tracks presented the standard value of 106 mils (50Ω characteristic impedance). The dimensions of test structures were 6120 X 3000 mils and the distance between test pads was 6000 mils. The PCB parameters were: FR-4 type, h= 60 mils, t= 17.5 μm, and εr= 4.66. Bellow are listed only some results obtained for a small via (12 mils) and for a large via (80 mils). The link with circuit simulators is based on the extracting RLCG parameters in SPICE format. After electromagnetic simulation, the above parameters extraction for all frequencies was done with “Modua”, a graphic display tool and a nodal circuit simulator inside Zeland environment. The results for 12 mils and 80 mils vias are in tables 2. 5 and 2. 6 presented.



a) b)

Fig. 2. 21 Current distribution in the spatial region of "via 12"
a) general view; b) zoom of the via

"Grid Generation" process has created 286 cells for "via 12" and 366 for "via 80". Simulation CPU times were: 87…97 s for "via 12" and 309…1100 s for "via 80".

Parameters→ Frequency (MHz) ↓	L_S (nH)	C_P (pF)
50	1.469	0.5186
100	1.468	0.5187
500	1.46	0.5205
800	1.452	0.523
1000	1.444	0.5252

Tab. 2. 5 Lumped LC Spice model for "via 12" (FR-4, h=60 mils, t= 17.5 μm, εr= 4.66)

Parameters → Frequency (MHz) ↓	L_S (nH)	C_P (pF)
50	1.261	0.4715
100	1.26	0.4715
500	1.248	0.4727
800	1.243	0.4745
1000	1.24	0.4759

Tab. 2. 6 Lumped LC Spice model for "via 80" (FR-4, h=60 mils, t= 17.5 μm, ε_r= 4.66)

Furthermore, modelling and simulation for evaluation of plasma and laser microvias were performed. A special laser/plasma ablatable dielectric material was selected, this being manufactured as resin coated copper (figure 2. 22b). Figure 2. 22a offers an image of a two coatings material (C-Staged: cured and B-Staged: semi-cured).

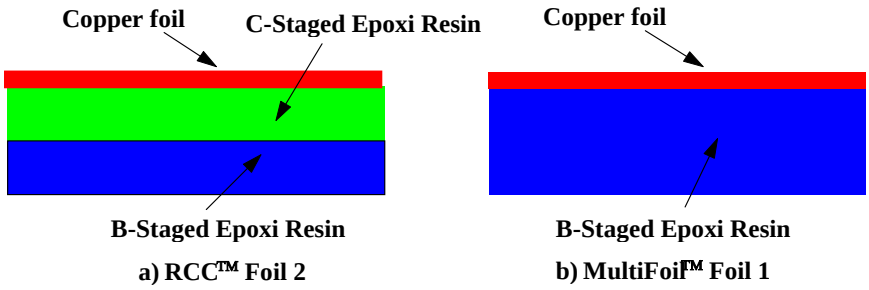


Fig. 2. 22 Resin coated copper materials for multilayer circuits

The analyzed structure (figure 2. 22b) consists in a single resin layer, coated once with a copper foil, in a semi-cured state. The resin has the properties both to fill and encapsulate the underlying circuitry and to offer the dielectric function. Usual values for this material are: B-Staged epoxi resin: 80 μm ≈ 3.15 mil, copper: 18 μm ≈ 0.71 mil, εr= 3.4 ... 3.6, tanδ= 0.025 ... 0.028. This material was placed on a conventional single sided FR-4 substrate with a ground plane onto the bottom side. Bellow are listed some results obtained for a plasma microvia (with the parameters: capture pads - 12 mils, via diameter on top - 7 mils, via diameter on bottom - 4 mils) and a laser microvia (with the parameters: capture pads - 8 mils, via diameter on top - 4 mils, via diameter on bottom - 3.5 mils). S-, Y-, and Z-parameters were obtained.

The link with circuit simulators through SPICE models was also done. In the same manner as for conventional vias, current distribution in the region of microvias and post-processed files for EMC evaluation of circuitry which contains microvias were prepared, too. Below are offered only the LC parameters tables.

Parameters→ ↓ Frequency (MHz)	L_S (nH)	C_P (pF).10^{-2}
50	0.8387	2.09
100	0.8374	2.09
500	0.8317	2.092
800	0.8299	2.096
1000	0.8289	2.099

Tab. 2. 7 Lumped LC Spice model for plasma microvia (B-Staged epoxi resin: 80 μm ≈ 3.15 mils, copper: 18 μm ≈ 0.71 mils, εr= 3.4 ... 3.6, tanδ= 0.025 ... 0.028 placed on a standard FR-4 structure, h=60 mils, t= 17.5 μm, εr= 4.66)

Parameters → ↓ Frequency (MHz)	L_S (nH)	C_P (pF).10^{-2}
50	0.9587	1.564
100	0.9569	1.564
500	0.9485	1.565
800	0.9459	1.568
1000	0.946	1.57

Tab. 2. 8 Lumped LC Spice model for laser microvia (B-Staged epoxi resin: 80 μm ≈ 3.15 mils, copper: 18 μm ≈ 0.71 mils, εr= 3.4 ... 3.6, tanδ= 0.025 ... 0.028 placed on a standard FR-4 structure, h=60 mils, t= 17.5 μm, εr= 4.66)

The main advantage of the newest type of micro-vias is that it is no more necessary to build the capture pad larger than the via. Practically, the pad diameter is equal to the trace width and with via diameter.

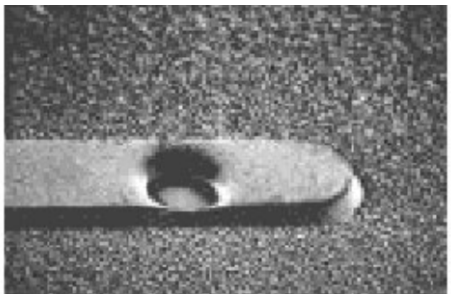


Fig. 2. 23 Micro-via generated into a copper trace (with no capture pad)