

5. Packaging Technologies Trends

Electronic products and microsystems continue to find new applications in personal, healthcare, home, automotive, environmental and security systems. Advancements in packaging co-design, low-cost materials and reliable interconnect technologies are critical in enabling the innovative packaging solutions required to help drive the industry forward (watch the presentation film below, created by IBM Research Laboratory, and observe some new trends in micro- and nanotechnology).



IBM Microelectronics Research Laboratory
(<http://www.youtube.com/watch?v=VsjzZaEWTgM>)

The tendency for miniaturization and implementation of HDI can be observed from figures 5.1.1 and 5.1.2.

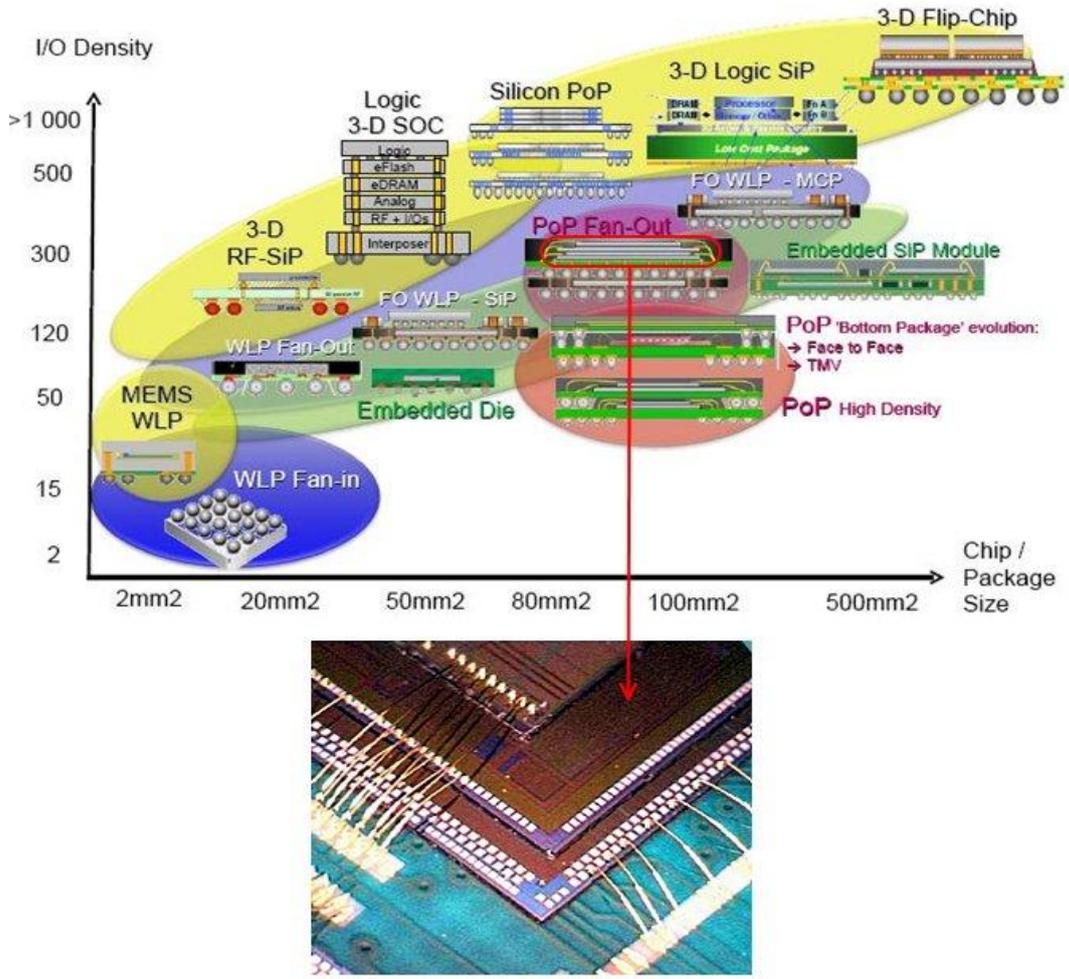


Fig. 5.1.1 I/O density of packages versus chip/package size (source: J. C. Eloy, EMPC 2009, Rimini)

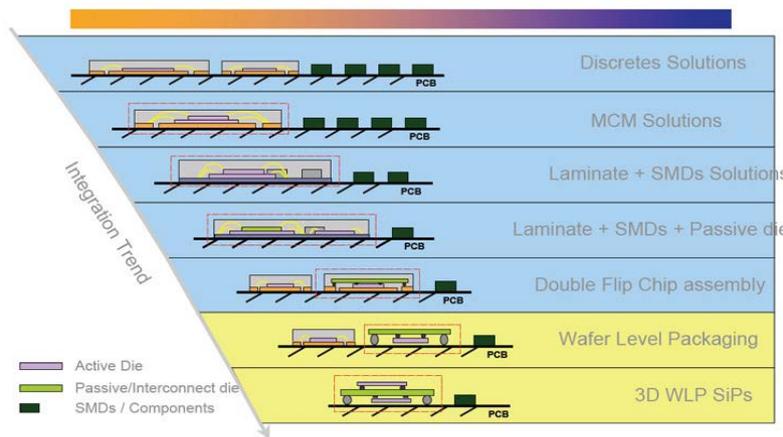


Fig. 5.1.2 Trends in packaging solutions

Packaging technologies trends reflect applications and end equipment in which they are integrated, as shown in figure 5.1.3. Among the many packaging challenges that must be addressed is the continuous development of powerful co-design tools used to shorten development cycles and enhance performance and reliability.

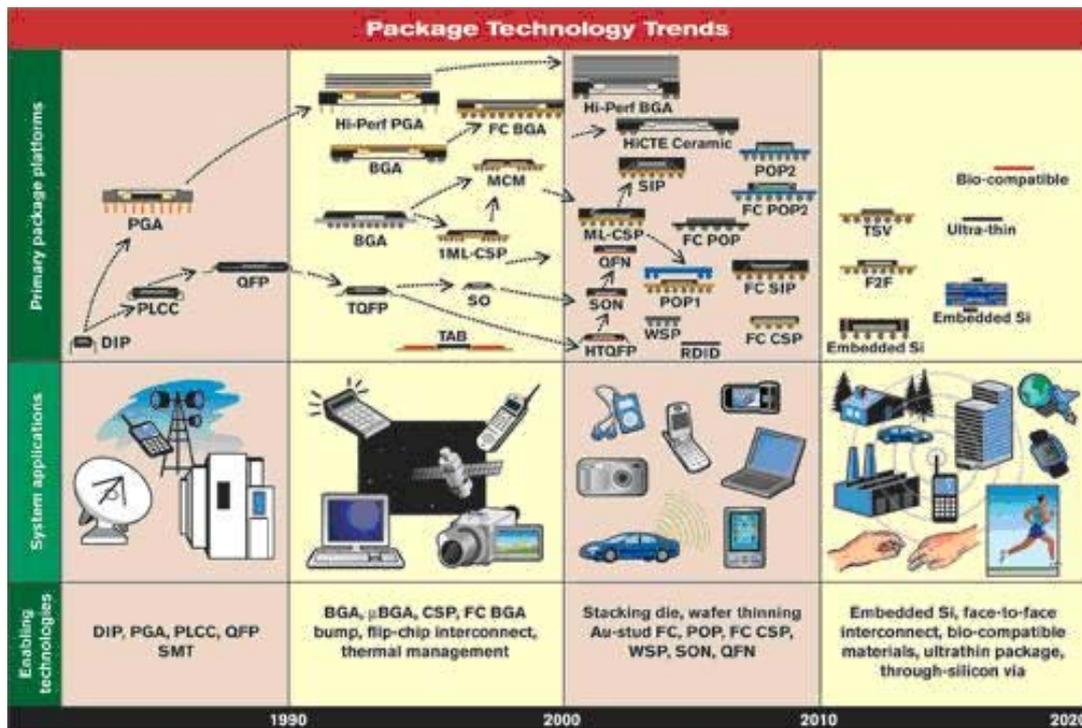


Fig. 5.1.3 Package technology and applications trends

Continuous pitch reductions and the use of 3D package interconnects in single-chip and multichip components, IC integration with sensors, energy harvesting and biomedical devices require packaging materials that are low cost and can be easily processed. Several challenges need to be addressed to support wafer-level bumping and lower-cost wafer chip-scale packages (WCSPs), focused on sub-60 μ m pitch bumping. And finally, we must be prepared to address unique packaging challenges of high-growth microsystems devices in automotive, portable handsets, consumer and medical electronics.

Electronic packaging is traditionally defined as the back-end process that transforms bare integrated circuits (IC) and schematic diagrams into functional products. As the IC feature size decreases and the size of silicon wafer increases, the cost per IC is reduced and the performance is enhanced. The future IC chips will be larger in size, will have more input/output terminals (I/Os), and will require higher power. In addition to the advancements in IC technology, electronic packaging is also driven by the market requirements for low cost, small size, and multi-functionality in the electronic products. In response to these requirements, packaging related areas such as design, packaging architectures, materials, processes, and manufacturing equipment are all changing rapidly. Wafer-level packaging (WLP) offers the benefits of low cost and small size for single chip packages, since the package is done at wafer level.

Moreover, after packages will reach the horizontal limit of dimensions, 3D stacking provides the solution and shall provide more efficient packaging through expanding packages

in the vertical dimension. Functional integration is achieved with 3D stacking architectures. As depicted in figure 5.1.4, 3D modules and systems are the way of the future, as they will be integrated in various electronic products and will have to address all current issues of signal integrity, robustness and reliability along with the general tendency for miniaturization.

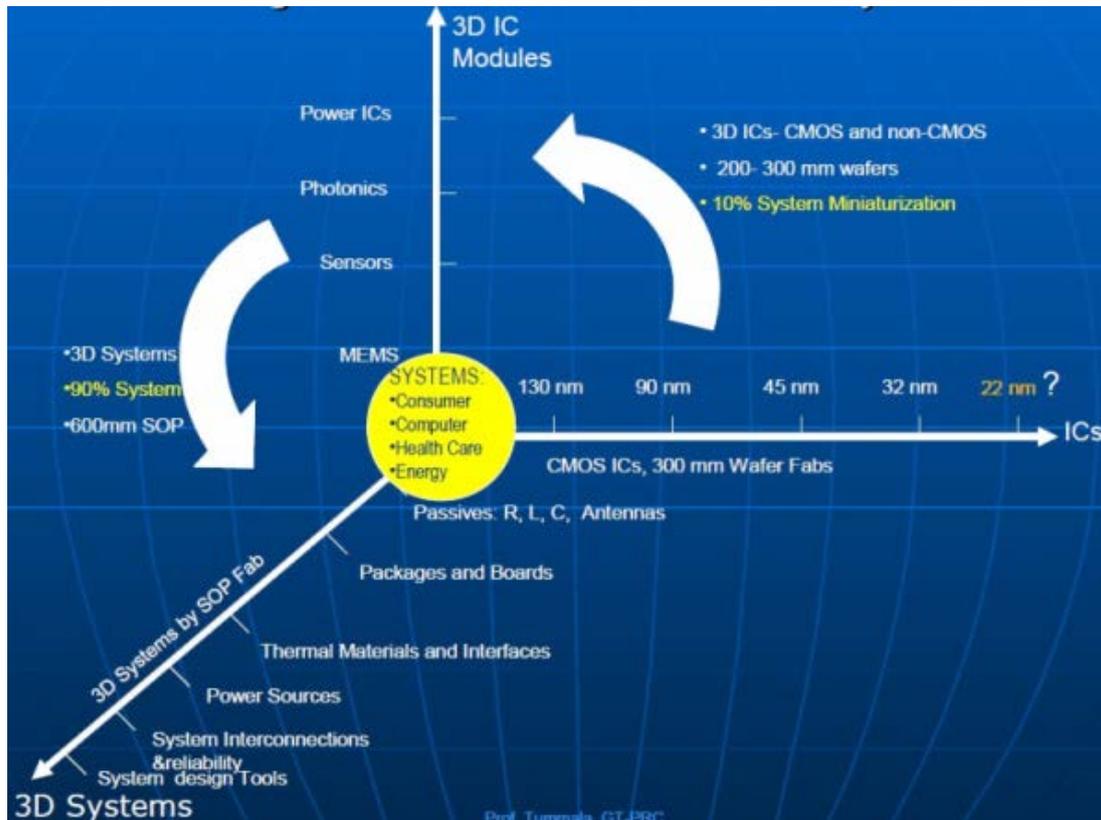


Fig. 5.1.4 Issues and Applications for small 3D systems and modules (source: R. Tummala, EMPC 2009, Rimini)

System-in-Package (SiP), one of the solutions to system integration, incorporates electronic and non-electronic devices such as optical devices, biological devices, micro-electro-mechanical systems (microsystems), etc., and supports interconnection in a single package to form smart structures or microsystems, devices which require specialized packaging to serve new market applications.

These trends, along with the emerging of a broad range of end equipment, require a large diversity of new IC package types to meet specific applications or markets as can be seen in figure 5.1.5. Increased device complexity will generate an explosion of new creative and disruptive technology packaging solutions, and in some markets and applications, packaging technology will become a key differentiator when making purchasing decisions.

To that end, there is a number of general packaging technology challenges the industry must address in the next years. Addressing the issues below will take the packaging technology roadmap to a new level, including migration towards ultra miniaturization, growth of package on package, modularization, package scaling to match silicon scaling,

nanostructures, 3D IC interconnect, optical input/interconnect and heterogeneous integration.

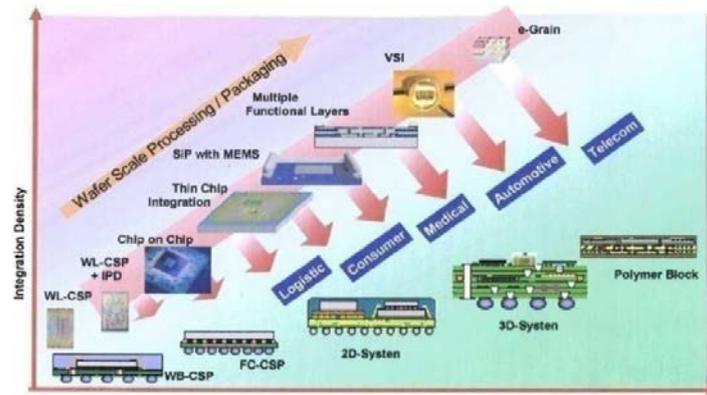


Fig. 5.1.5 Applications on the market of complex packages

Packaging advanced CMOS technology with copper and ultra low-k dielectrics

The biggest challenge impacting packaging in the next years is the industry's ability to develop packaging solutions for both advanced CMOS with copper and ultra-low k dielectrics. The fast adoption and high volume ramp of advanced CMOS silicon with copper interconnect and low k dielectrics have had a major impact on packaging. Packaging must move toward compliant chip-to-chip substrate interconnects and low stress packaging solutions, along with mechanical reinforcements under pads. The ability to perform better characterization is essential, along with development of interconnect ILD materials to address interfacial adhesion and improve fracture toughness. Thermal connectivity with strained silicon is potentially 4...5 times worse than bulk silicon. The industry needs to better understand this issue and address potential problems. Developing wafer thinning and dicing solutions for wafers with copper and ultra-low k dielectrics will also be required.

Scaling for More Die Per Wafer and New Interconnect Technology

Disruptive packaging solutions will be necessary to continue to scale down size and area for product input/output, and pad ring in CMOS nodes beyond the 32-nm process. An estimation of size reduction and complexity increase can be observed in figures 5.1.6 and 5.1.7.

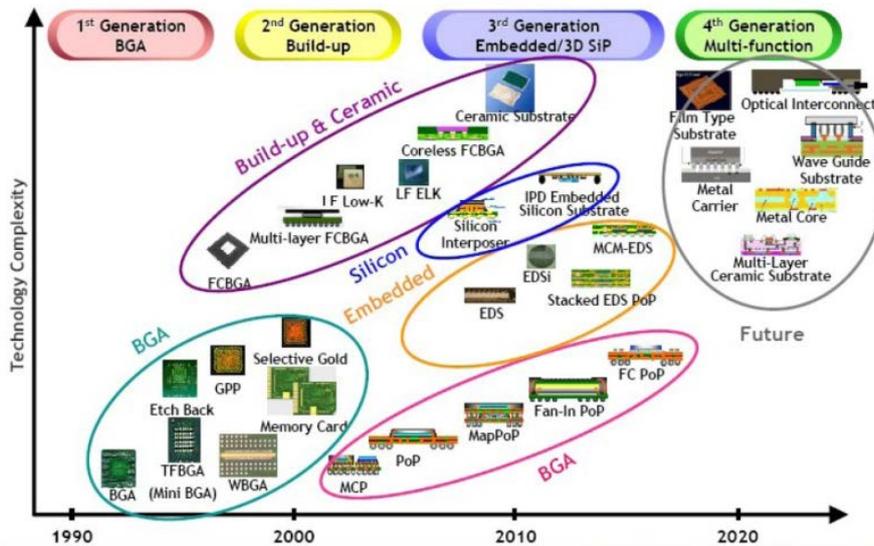


Fig. 5.1.7 Timeline for package complexity increase (source: J. C. Eloy, EMPC 2009, Rimini)

In addition, ultra fine pitch and compliant interconnect solutions such as micro-bumps, coated-wire bonding process, fine pitch less than 50µm wire bonding and Au stud bumping to thinned dies will also be needed in this time frame. Some may consider whether the industry will see the end of solder bump for ultra fine flip chip interconnect applications. Other technologies that will be explored are room temperature Cu-Cu interconnection and fine pitch pad alignment, 3D IC Interconnect, wafer-to-wafer, die-to-wafer, through silicon vias, and Cu nails. The tendency for stacking in the area of interconnects can be observed in figure 5.1.8.

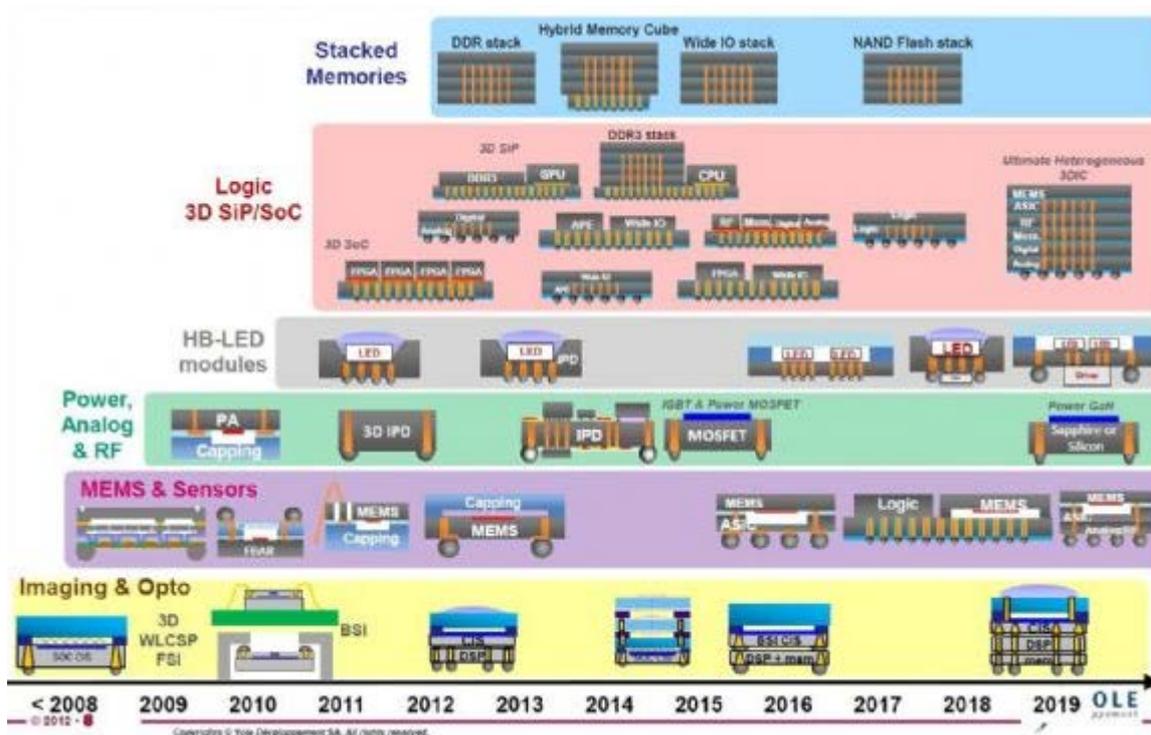


Fig. 5.1.8 3D-TSV interconnects technology roadmap (source: J. C. Eloy, Yole Development, 2012)

SoC and SiP Integration and Functionality, Automated System Level Co-Design Tools

Product designers are continuously facing the question of whether they should design new products using SoC or SiP, or both. This is especially true in the mobile handset market where consumers are increasing their reliance on the handset to listen to music, take and send pictures, record and watch videos, play games and more, which can also be seen from figure 5.1.9 presented by Nokia. Operating multiple applications places an increased strain on system memory requirements and is driving the need for SiP solutions. Functionality increases with time for SiP and SoC, and cost is typically the deciding factor for SoC vs. SiP at a given time.

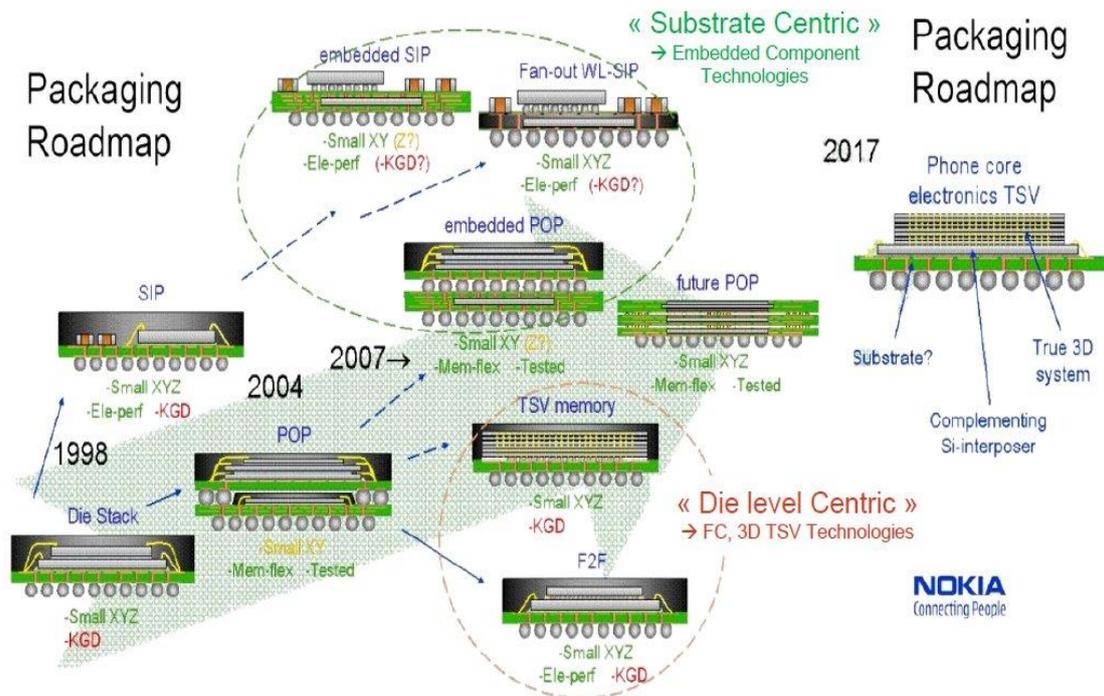


Fig. 5.1.9 Packaging roadmap in the development of mobile handsets

Another critical gap the industry must close is faster development and availability of 3D Chip-Package-System Co-Design Automation for electrical, thermal and mechanical compatibility. Development of cost-effective package-on-package modules is also critical, along with the impact to manufacturing business models and testability.

The industry is also experiencing challenges in rolling out complex SoC products that include RF and analog integration around digital cores. Digital and RF integration into smaller modules requires closer placement of the digital and RF dies, a necessity that lead to the significant increase of components per package in less than a decade, as can be seen in figure 5.1.10.

This has raised interference issues between the digital and RF signals that must be resolved, and integrated shielding and flip chip solutions could help address the issues. Modelling tools with more predictable results are essential, with the ability to allow virtual packaging of advanced silicon and systems. System and component level reliability failure

modes and acceleration factors must be well understood, and there will be an increased need for modelling and design tools to predict manufacturability and reliability performance.

Revenue forecast by advanced packaging platform From 2014 to 2020, in US\$ million

(Source: Status of the Advanced Packaging report, Yole Développement, November 2015)

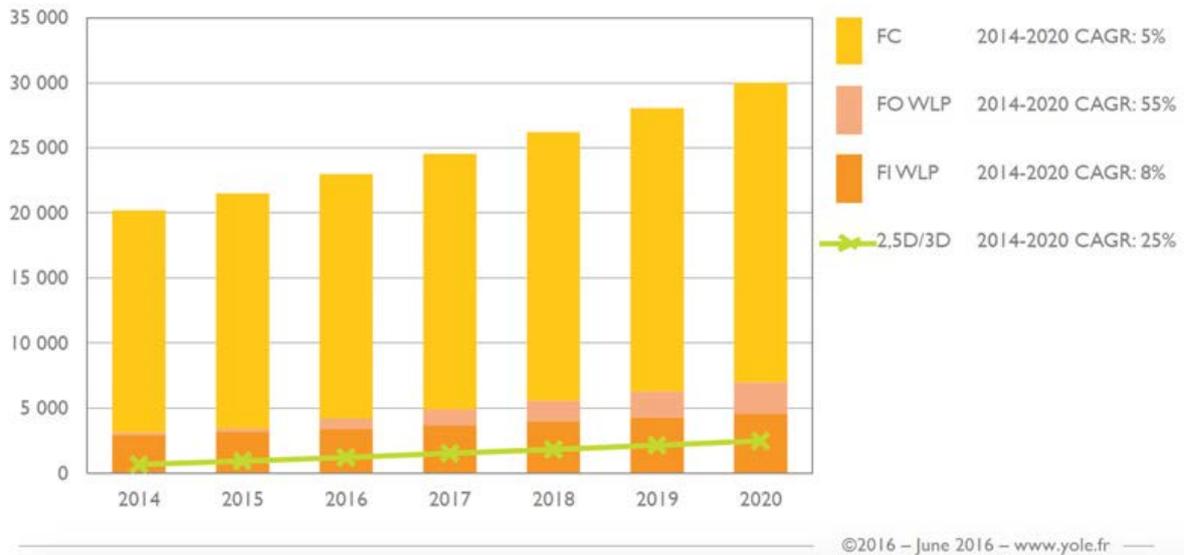


Fig. 5.1.10 Overall package unit growth over less than a decade

Higher Performance and Higher Thermal Density

A change from the use of wide/slow busses to high speed serial I/O will drive the need for low cost, matched transmission line characteristic packages, and new thermal management techniques will be implemented to address cooling. Some companies are currently exploring methods such as RF shields, and expect those to become an integral part of packaging for future consumer electronics and portable products. Techniques such as the use of heat pipes and vents will ultimately migrate toward use in these systems and move heat to the system enclosure. Additionally, Multi-Core Microprocessors will drive die size up and increase demands for high performance multi-chip modules. Non-traditional thermal management solutions, such as liquid cooling, compact and solid state refrigeration will be needed but at significantly lower costs.

The industry is experiencing increased demand for low-cost, high-performance packages, and development of high-performance wire bond and low-cost flip chip packaging is essential. A better understanding of fundamental issues related with lead-free packaging, for example, and metallurgical life prediction models will aid on this front. In addition, hot spot minimization will drive a need for a high thermal conductivity die attach directly to Cu spreading plates in organic substrate BGA packages. As a result, flip chip packaging portfolios and volumes will grow significantly.

New Packaging Materials

In the next years, development of several new packaging materials is critical. Some examples include low stress underfill to support large die sizes, ultra fine pitch bump and more than 10K bumps/die. Pressurized underfill is one technique showing strong promise. Vacuum underfill solutions for small die are also under evaluation, and there is potential for extended use for large die. These solutions, however, do not do much to enhance current technology-capillary fill. No flow and wafer-level fill hold much promise for large, high bump count devices, so some additional driving force is necessary for successful fill-vacuum and/or pressure.

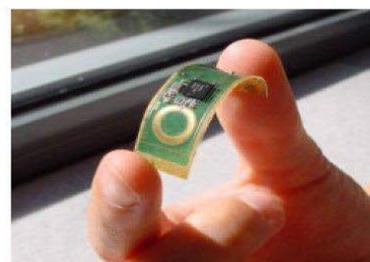
Thermal stability is a key issue, especially in the automotive environment, and the current material set, and perhaps the fundamental epoxy chemistry, will not meet requirements for 180°C continuous operations. Exploration of high junction temperatures, >150°C, mold compound and die attach materials, is underway as a solution to the challenge. This issue extends to RF modules as power density in RF devices is expected to increase dramatically over the next years while the size continues to shrink. Highly conductive mold compounds and encapsulates used to support RF modules have the potential to help maintain thermal conductivity despite these changes.

Package substrates will also require considerable development and improvement, especially in high speed electrical transmission applications. For example, silicon substrate can reduce the size of transmission line and line width through the use of lithography technology, and a minimum size transmission line can reduce resistance leading to high speed applications. Some other techniques that may prove successful include coreless thin substrates (wire bond and flip chip) with reduced metal layers to support thin packages and stacked die packages. Substrates with selected solder pre-coating and thin Ni-Au plating areas are another alternative.

Large format substrates are experiencing manufacturability, warpage and board attach issues, and these need to be addressed. A very critical requirement is development of low-cost fine pitch flip chip substrates to achieve cost parity with wire bonded packages. This could be achieved by increasing wiring density per layer and reducing layer count, which will lead to the development of small stacked packages and devices for general use which are easy to carry and manipulate as the ones depicted in figure 5.1.11.



3 D integration
Small footprint



2 D integration:
Thin and flexible
Stick on skin, integrate in cloth

Fig. 5.1.11 2D and 3D integration (source: IMEC)

There is also an emergence of lead-free and RoHS-compliant packaging and use of lead-free solders and 'green materials'. To address thermal requirements, new and exotic lid and lid attach materials will be developed. Solder lid attach, high-k lids, micro-channels in the Si or lids and other solutions must have low resistance and excellent reliability for adoption in future packages.

New Assembly Processes

Many new assembly processes will be developed and implemented during the next years, including ultra thinning of wafers < 50µm to enable stacked die, package on package, and ultra thin package. New technology such as laser dicing may be needed, and one example is dicing of advanced Si wafers with low-k dielectrics. Wafer level packaging to improve reliability and pin count, ball pitch and routability, are also imperative. New under bump metallurgy, bump structure, pre-applied underfill are potential alternatives to improve reliability.

Also important is an understanding of the limitations of wire bond technology in high junction temperature type of applications. For example, 150°C Tj is likely the limit for gold wire on aluminium bond pads. New solutions, including different wire alloys and bond pad metal system, need to be explored along with new encapsulation processes. Liquid compound, compression molding, wafer level molding and low stress thin package encapsulation technologies are examples of low stress assembly processes that combined with low force wire bond and no damage multi probing may be needed to support the assembly and packaging of new CMOS copper and ultra low-k silicon processes.

In conclusion, advanced technologies shall continue to deliver highly differentiated and integrated SoC and SiP solutions with high performance, high thermal density, low power and low cost. Development of packaging solutions with a cost structure that follows and matches the silicon cost reduction learning curve is the key to success. The tendency is to maximize the use of standard and commercially available high volume processing, even if this means that the design has to be changed or additional steps must be introduced. This trend is inadvertently leading to the reliance on thinner wafers and 3D packaging, both requiring processes such as wafers thinning, microvia creation and new technologies for die separation.

Additionally, wafer scale packaging is becoming a key enabling technology, bringing front and back-end processing together. This technology and the related technologies of 3D packaging are of increasing importance in microsystems. On a longer time scale, thin film encapsulation will partly replace wafer bonding, while it makes thinner packages easier to create. Although microsystems have decreased in size over the years, it hasn't decreased as much as the surrounding electronics. This will become another key point of attention. For monolithic processing, decreasing the microsystem structures to dimension in the same size range of CMOS structures shall be also of the highest interest.